[ENG81]

UNIVERSITY OF GREATER MANCHESTER

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER 2 EXAMINATIONS 2024/25

INTERMEDIATE DIGITAL ELECTRONICS AND WIRELESS COMMUNICATIONS

MODULE NO: EEE5012

Date: Thursday 15 MAY 2025 **Time: 14:00 – 16:30**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.
Answer any FOUR questions.
All questions carry equal marks.
Marks for parts of questions are shown in brackets.
This examination paper carries a total of ONE HUNDRED marks.
All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

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Question 1

A. You are tasked with designing a digital control system for an automated machine that receives three binary inputs — x, y, and z — and produces a single output, F. The three inputs represent sensor readings, and the output F controls the operation of a mechanical component (e.g., a motor, blade, or actuator).

The system operates under different conditions, and the behaviour of the machine is defined by how F responds to the combination of inputs. The output F will determine whether the mechanical component activates (when F = 1) or remains inactive (when F = 0).

Design the combinational circuit that satisfies the following conditions:

i. The machine should activate (**F = 1**) if the binary value formed by the inputs (**xyz**) is **less than 3**. If the binary value is **3 or greater** (011 to 111), the machine remains inactive (**F = 0**).

[9 marks]

ii. The machine activates (**F = 1**) if the binary value of (**xyz**) is an **odd number**. If the binary value is **even**, the machine remains inactive (**F = 0**)

[4 marks]

B. Develop a circuit design for an advanced digital electronics system with three input signals (x, y, z) and three output signals (A, B, C). The circuit should function as follows:

For binary inputs 000 to 011 (0 to 3 in decimal), the output should be the binary equivalent of the input value plus two and for binary inputs 100 to 111 (4 to 7 in decimal), the output should be the binary equivalent of the input value minus two.

[12 marks]
[Total - 25 marks]
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Question 2

Consider the Combinational circuit shown in Figure 2.

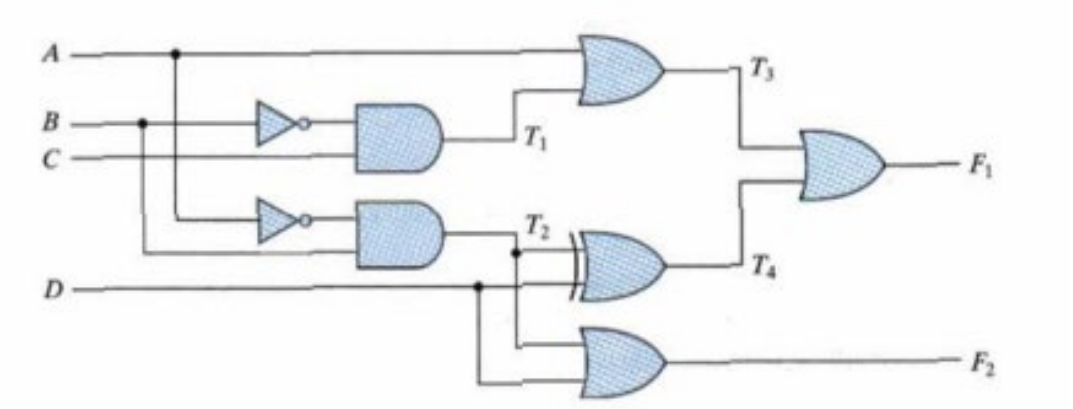

Figure 2

a) Derive the Boolean expressions for T1 through T4. Evaluate the outputs as a function of the four inputs.

[9 marks]

b) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T1 through T4 and outputs F1 and F2 in the table.

[16 marks]

[Total - 25 marks]

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Question 3

A. The D latch of Figure 3 is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch, and in each case draw the logic diagram and verify the circuit operation:

a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed. Properly label all inputs and outputs.

[6 Marks]

b) Use NOR gates for all four gates. Inverters may be needed. Properly label all inputs and outputs.

[6 Marks]

c) Design the function table for the D-Latch.

[3 Marks]

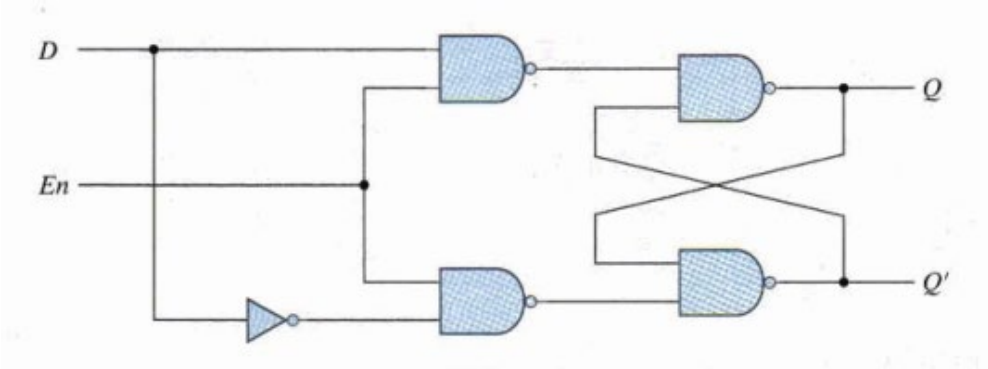

Figure 3

B. Design a 4-bit adder-subtractor circuit capable of performing binary addition and subtraction on two 4-bit inputs, A and B using a mode selector. Present a clear schematic that integrates full adders and necessary logic gates. Explain the function of the mode selector, detailing how the circuit processes both operations and manages carry/borrow bits across the full adders. Your explanation should elucidate the binary arithmetic performed by the circuit for each mode.

[10 marks]

[Total - 25 marks]

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Question 4

A. As a digital system engineer testing a new state machine, you are tasked to verify its transition logic. Refer to the state diagram provided in Figure 4, with an initial state of 00. Analyze and document the state transitions and the corresponding output sequence that the system will generate when the input sequence 010111100011110 is applied. Detail each transition and output clearly for assessment.

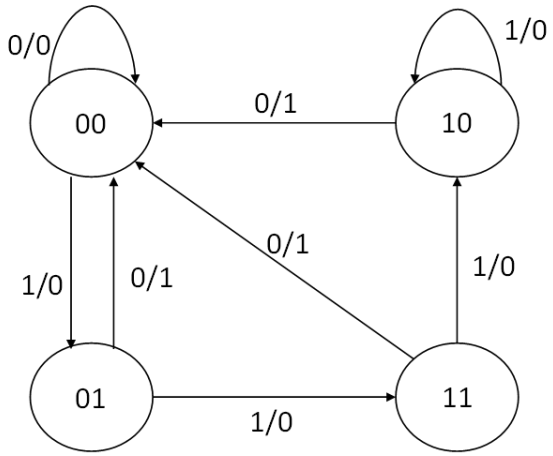

Figure 4: State Diagram

[15 Marks]

B. Reduce the number of states in the following state table and tabulate the reduced state table.

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

[10 marks]

[Total – 25 Marks]

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Question 5

Using a fully illustrated diagram of a 4-bit full-adder circuit, design and determine how a digital electronic circuit compute

a) 8 – 6

[13 marks]

b) 8 + 6

[12 marks]

Be sure to indicate the control signal (mode) bit, minuend bits, subtrahend bits and sum bits in each case.

[Total = 25 marks]

Question 6

A. Design an Orthogonal Frequency Division Multiplexing (OFDM) transmitter and receiver. Provide a detailed schematic and clearly label each component.

[10 Marks]

B. In digital electronics and communications, modulation is the process of modifying a carrier signal to encode information. Three common modulation techniques are amplitude modulation, phase modulation, and frequency modulation.

   i. Briefly explain the principle of amplitude modulation, describe how the amplitude of the carrier wave is varied in proportion to the message signal and sketch a representative graph of an AM signal.

   [7.5 marks]

   ii. Briefly explain the concept of phase modulation, describe how the phase of the carrier signal is varied according to the instantaneous amplitude of the message signal and sketch a representative graph of a PM signal.

   [7.5 marks]

[Total - 25 marks]

END OF QUESTIONS