

UNIVERSITY OF GREATER MANCHESTER
SCHOOL OF ENGINEERING
BENG (HONS) ELECTRICAL AND ELECTRONIC
ENGINEERING
SEMESTER 2 EXAMINATIONS
2024/2025
INTRODUCTORY DIGITAL ELECTRONICS
MODULE NO: EEE4013

Date: 12 MAY 2025

Time: 10:00 – 12:00

INSTRUCTIONS TO CANDIDATES:

There are **SIX** questions.

Answer any **FOUR** questions.

All questions carry equal marks.

Marks for parts of questions are shown
in brackets.

This examination paper carries a total of
100 marks.

All working must be shown. A numerical
solution to a question obtained by
programming an electronic calculator
will not be accepted.

Question 1

a) A manufacturing plant uses 2 tanks to store certain liquids, see system diagram partially presented in Figure Q1.a. Each tank has a sensor that activates when chemical level drops off to 25% of full. The sensors produce a HIGH level of 5V when the tanks are more than one-quarter full, in case the level is below 25% the signal is LOW of 0V. It is required that a single green LED on a panel shows when both the tanks are more than 25% full.

- (i) Use digital electronics knowledge to analyse the system requirement and write down the truth table.

[5 marks]

- (ii) Based on your analysis, decide which logic gate would be suitable to meet the system requirement and complete the system diagram

[3 marks]

- (iii) The manufacturer now decides to modify the system so that the green LED will be ON if one and only one of the tank is below 25%. Redesign the circuit for the system with suitable logic gate and list the truth table.

[7 marks]

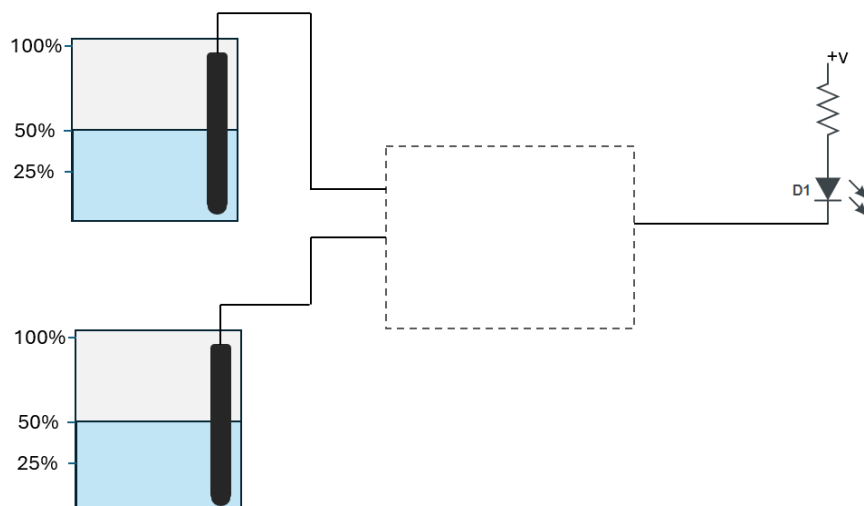


Figure Q1.a System diagram

Question 1 continues on the next page...

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- b) Map the following Boolean Expression into Karnaugh map and produce a minimum SOP (Sum of Product) form.

$$\overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + ABCD + ABC\overline{D}$$

[10 marks]

Total 25 marks

Please turn the page

Question 2

a) Solve the following and provide the answer in the required bases.

i) $11110_2 \times 10010_2 = \underline{\hspace{2cm}}_2 = \underline{\hspace{2cm}}_{\text{Hex}}$

ii) $1100_2 - 0110_2 = \underline{\hspace{2cm}}_2 = \underline{\hspace{2cm}}_{10}$

iii) $1011_2 + 1100_2 = \underline{\hspace{2cm}}_2 = \underline{\hspace{2cm}}_{10} = \underline{\hspace{2cm}}_{\text{Hex}}$

[14 marks]

b) You are going to use a shaft encoder to track the current position of a rotatory motor, and the encoder implement Gray code rather than the Binary code. Explain the difference between the Gray code and Binary code, and what is the advantage of using Gray code?

[4 marks]

c) Figure Q2.a1 is a 2-bit comparator with one output $A=B$. The timing waveform of 4 inputs are shown in Figure Q2.a2, determine and draw the timing waveform below at the output ($A=B$).

[7 Marks]

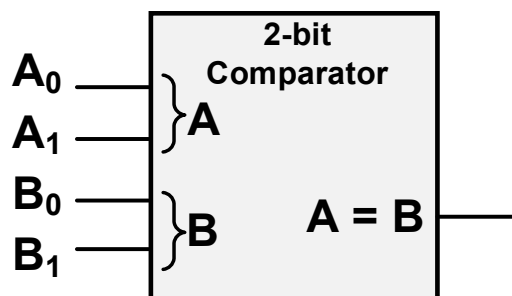


Figure Q2.a1: 2-bit Comparator

Question 2 continues on next page...

Question 2 Continues

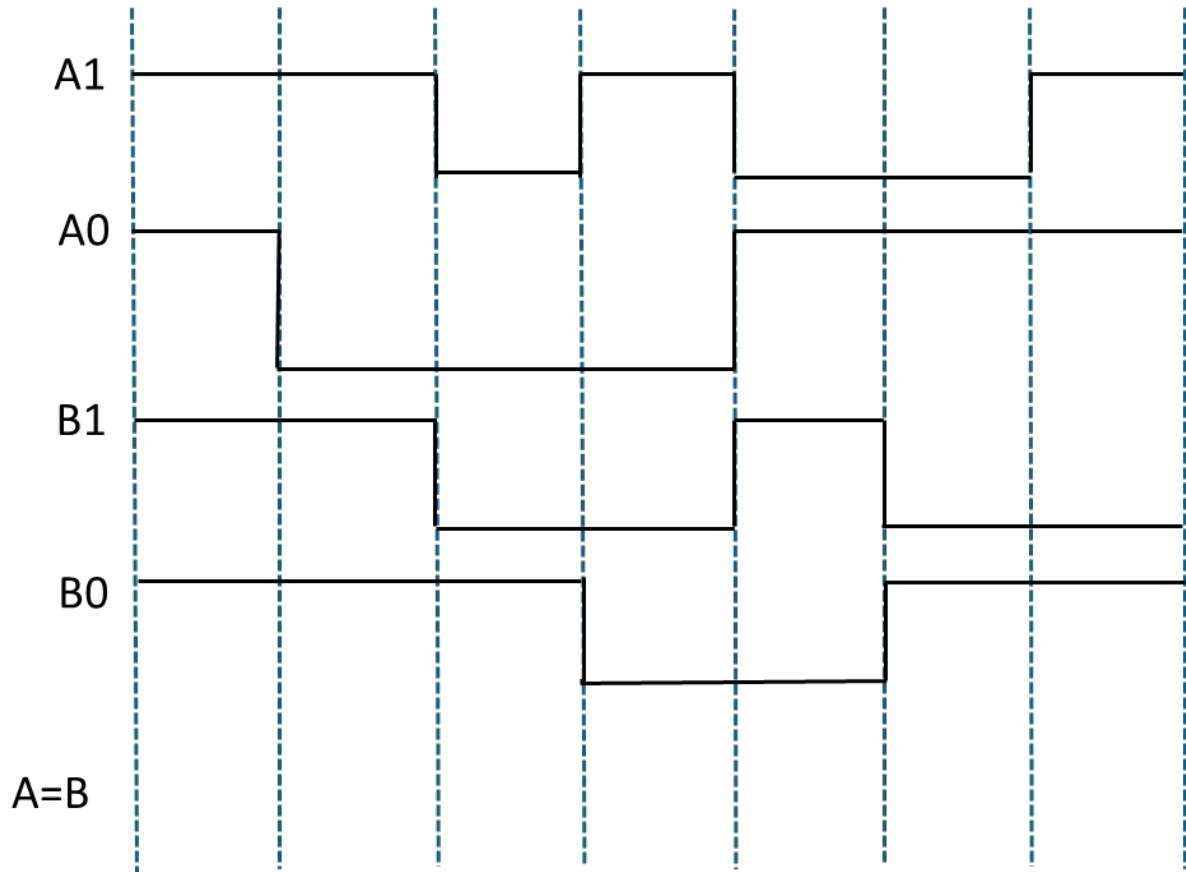


Figure Q2.a2: Comparator Timing Waveforms

Total 25 marks

Please turn the page

Question 3

- a) With the aid of diagrams, explain the difference between a combinational logic circuit and a sequential circuit. List one application example for combinational logic circuit and sequential circuit, respectively.

[12 marks]

- b) Determine the sum generated by the 3-bit adder shown in Figure Q3.b below, as well as the output carriers C_1 , C_2 and C_3 when binary numbers 110 and 101 are added with input carrier $C_0 = 0$.

[5 marks]

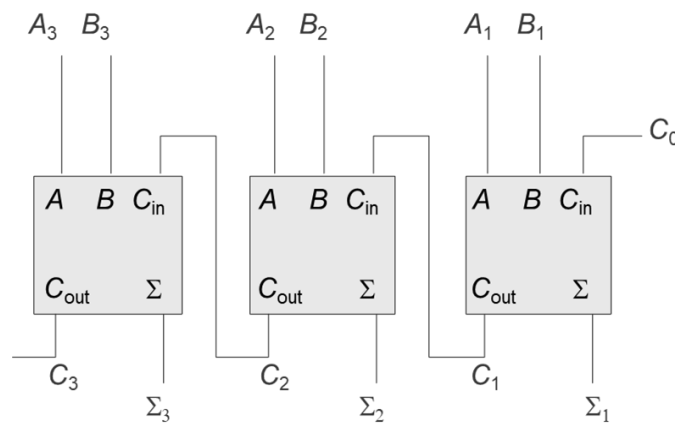


Figure Q3.b 3-bit adder

- c) Draw the waveform of output Q of a positive edge-triggered J-K-flip flop, the input waveforms are provided in Figure Q3.c.

[8 marks]

Question 3 continues on the next page...

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Question 3 Continues

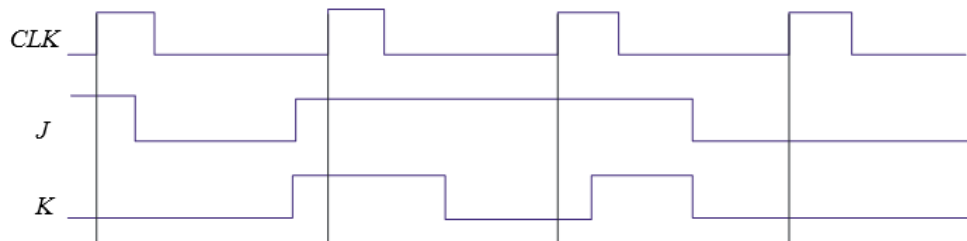


Figure Q3.c JK Flip Flop input Waveforms

Total 25 marks

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Question 4

A logic diagram is shown below in Figure Q4

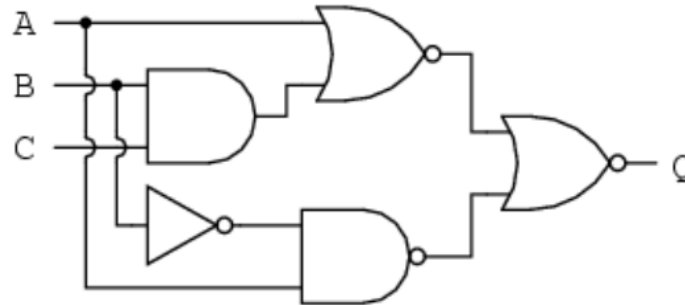


Figure. Q4 Logic circuit diagram with 3 inputs A B and C and output is Q

- Work out the Boolean expression from this circuit
[5 Marks]
- Use Boolean Algebra to simplify the expression you obtained from a)
[8 Marks]
- The 3 inputs will have 8 possible states. Complete the below truth table in Table. Q4
[6 Marks]
- If the state 0 is the least significant bit and state 7 is the most significant bit. Convert the output column as an 8-bit binary code first, and then convert it to decimal, and hexadecimal code, respectively.
[6 Marks]

Table.Q4, Truth table with 3 inputs and 1 output

	A	B	C	X (output)
State 0	0	0	0	
State 1	0	0	1	
State 2	0	1	0	
State 3				
State 4				
State 5				
State 6				
State 7				

Total 25 marks

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Question 5

- a) Describe the three differences between synchronous and asynchronous counters.

[6 marks]

- b) Using J-K flip-flops, design a 2-bit up asynchronous counter and your design should include

- i. A circuit diagram using J-K flip-flops

[4 Marks]

- ii. A truth table showing the counter sequence

[5 Marks]

- c) If the 5-bit ripple counter has a 500-kHz clock signal applied.

- i. What is the MOD (modulus of a counter) number of this counter?

[5 marks]

- ii. What will be the frequency at the MSB (most significant bit) output?

[3 marks]

- iii. What will be the duty cycle of the MSB signal?

[2 marks]

Total 25 Marks

Please turn the page

Question 6

- a) An 8-bit serial in/serial out shift register has a 50 MHz clock. What is the total delay through the register?

[5 marks]

- b) For the circuit shown in Q6 b, What's the purpose of the 'Load control-LD' in the registers?

[4 marks]

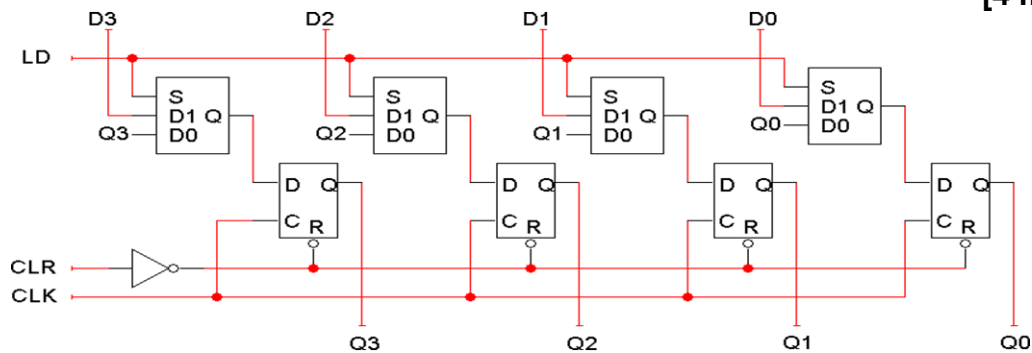


Figure Q6b Circuit diagram of register with LD control input

- c) Fig.Q6c is a 4-bit shift-left register (uses D-flip-flops). Considering starting with setting Q3 Q2 Q1 Q0 outputs to 0110, and data input SI is steady logical 0, decide what will be the new value after one active clock edge.

[5 marks]

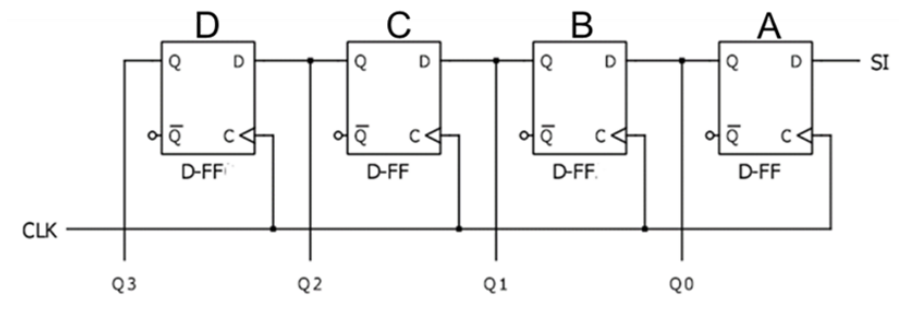


Figure Q6C Circuit diagram of 4-bit shift-left register

Question 6 continues on next page...

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- d) For the multiplexer circuit shown in Q6d, if $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, $D_3 = 0$, $S_0 = 1$, $S_1 = 1$, $\overline{EN} = 0$.
- What is the status of the Y output?
 - What's the purpose of \overline{EN} pin in the multiplexer?

[6 marks]

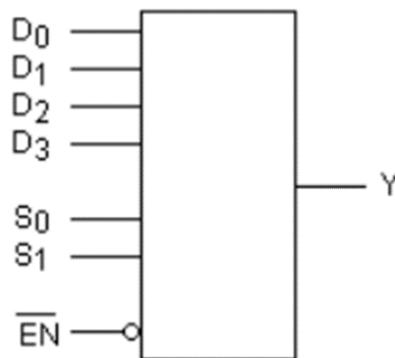


Figure Q6d Multiplexer Circuit

- e) Assuming the output of the decoder shown below (Fig. Q6e) is a logic "1". What are the inputs to the Active HIGH decoder and the logic expression of the decoder?

[5 Marks]

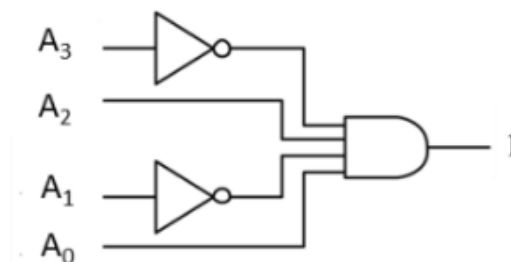


Figure Q6e Circuit Diagram for one decoder

Total 25 Marks

END OF QUESTIONS

Please turn the page for the Formula Sheet

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Formula sheet

Commutative Law of Boolean Algebra

$$A + B = B + A$$

$$AB = BA$$

Associative Law of Boolean Algebra

$$A + (B + C) = (A + B) + C$$

$$A(BC) = (AB)C$$

Distributive Law of Boolean Algebra

$$AB + AC = A(B + C)$$

Rules of Boolean Algebra

$$1. A + 0 = A$$

$$2. A + 1 = 1$$

$$3. A \cdot 0 = 0$$

$$4. A \cdot 1 = A$$

$$5. A + A = A$$

$$6. A + A = 1$$

$$7. A \cdot A = A$$

$$8. A \cdot A = 0$$

$$9. A = A$$

$$10. A + AB = A$$

$$11. A + AB = A + B$$

$$12. (A + B)(A + C) = A + BC$$

DeMorgan's Theorems

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

END OF EXAM