ENG37

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

MSC SYSTEMS ENGINEERING AND ENGINEERING MANAGEMENT

SEMESTER 2
EXAMINATION 2023/2024

MICROPROCESSOR BASED SYSTEMS

MODULE NO: EEM7016

Date: Thursday 16th May 2024 **Time: 10:00 – 12:00pm**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

Answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Electronic calculators may be used provided that data and program storage memory is cleared prior to the examination.

CANDIDATES REQUIRE: **PIC18F452 data sheet (attached).**

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Question 1.

a) Describe the registers' operation of the Input/Output (I/O) port of the PIC18F452 shown in Fig.1.

(6 marks)

b) Use the I/O block diagram shown in Fig.1 to configure the port noted as an Input/Output (I/O) pin for input.

(7 marks)

c) Use the Input/Output (I/O) block diagram shown in Fig.1 to configure the port noted as I/O pin for output High (HI).

(7 marks)

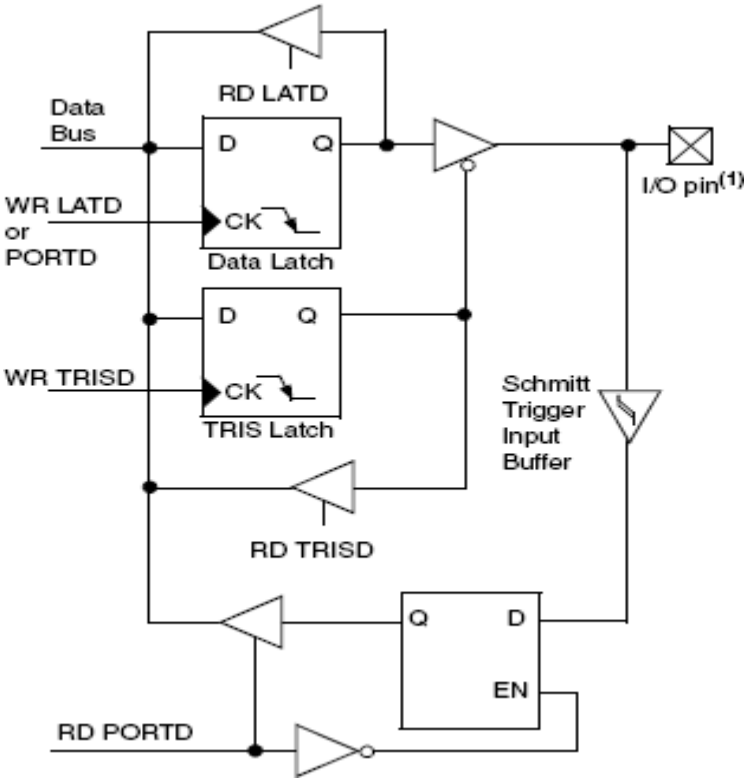

Fig.1: Showing the I/O block diagram.

d) Explain how to use Read/Modify/Write Bit-wise operators to set Bit-2 without changing other bits by assuming the initial value of LATD register is 01101001.

(5 marks)

Total 25 marks

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Question 2.

a) Describe the differences between the following codes: Machine Code, Assembly Code, and 'C' Code.

(6 marks)

b) What is the difference between a 'while' loop and a 'do while' loop in 'C'? Explain this difference in terms of the execution methodology and code syntax of each one.

(4 marks)

c) Write a function in C language named min () that returns the minimum value of three arguments that are passed to the function when it is called. Assume that all three arguments will be of the float data type.

(7 marks)

d) Write a program in C language to add two matrices A[4][3] and B[4][3].

(8 marks)

Total 25 marks

Question 3.

Part A - Select the correct choice below – maximum of 12 marks

1) A flowchart is a method to describe the software design where the rectangular symbol refers to

(2 marks)

i. an instruction or a command.
ii. a decision statements.
iii. a jump from one point in the sequence to another.
iv. a point where there is input to or output from the program.

2) The width of the data bus can be measured directly based on the (2 marks)

i. largest number that the bus can carry.
ii. smallest number that the bus can carry.
iii. amount of memory a system can retrieve.
iv. data and Instructions through the bus.

3) The PIC18F452 microcontroller device has (2 marks)

i. three bidirectional programming data ports.
ii. four bidirectional programming data ports.
iii. five bidirectional programming data ports.
iv. six bidirectional programming data ports.

Q3 Part A continues over the page
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Q3 Part A continued

4) The steps order of the software part of the embedded system design is (2 marks)

i. Code the design, compile the code, algorithm design, program code to target, run the target and test.
ii. Algorithm design, code the design, program code to target, compile the code, run the target and test.
iii. Algorithm design, compile the code, code the design, program code to target, run the target and test.
iv. Algorithm design, code the design, compile the code, program code to target, run the target and test.

5) One of the reserved keywords in C programming language is: (2 marks)

i. try
ii. throw
iii. catch
iv. case

6) The incorrect identifier name of a variable in C language is (2 marks)

i. B6
ii. b6.13
iii. OK_
iv. X_ray

Part B - Write the required code to configure the LCD function shown in Fig.2 to perform the following commands: - maximum 13 marks

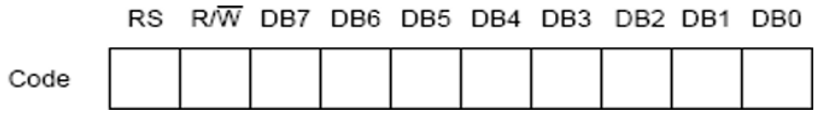

Fig.2: Showing LCD configuration.

1. Display on/off control (5 marks)
2. Clear display (2 marks)
3. Return home (2 marks)
4. Write data (2 marks)
5. Read data (2 marks)

Total 25 marks

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Question 4.

a) Draw a state machine diagram for a simple children's moving toy. The toy moves in response to sound and stops when it touches an object. The specifications are as follows:

- The toy is switched on using a button click to **Start**.
- After turning it on the toy is **Idle**.
- If a sound is detected (label it as: "On Sound"), the toy will **Start Motor Forward**.
- It then carries on **Moving Forward** until it either touches an object (label it as: "On Touch") which then causes it to **Stop** or if another sound is detected, the toy should **Start Motor Backward**.
- Again, the toy continues **Moving Backward** until it either touches an object (label it as: "On Touch") which causes it to **Stop** or if another sound is detected (label it as: "On Sound"), the toy will **Start Motor Forwards** again.

When the toy is stopped, it will then move to the **Idle** position and **Start Motor Forward** if a sound is detected. (12 marks)

b) Write a C code function under the name "StateMachineToy" using switch case statement for implementing the state machine diagram that you created in part-a.

(13 marks)

Total 25 marks

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Question 5.

a) Write a C program to draw star-pattern of the shape below: (13 marks)

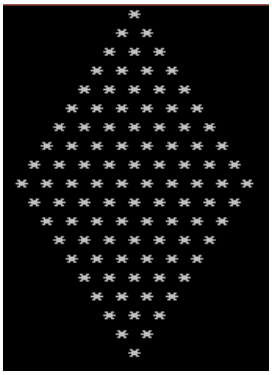

Fig.3: Showing a star-pattern of diamond.

b) What is the role of the data and address bus in a computer Central processing Unit (CPU)? (4 marks)

c) Compare the difference between Von-Neumann and Harvard architectures in terms of:

1. Memory organisation (4 marks)
2. Advantages (2 marks)
3. Disadvantages (2 marks)

Total 25 marks

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Question 6.

a) The PIC18F452 has a 16-bit timer but the data bus is only 8-bits wide. Explain how a 16-bit timer read/write is carried out. (10 marks)

b) The timer module of a PIC18F452 is configured as given below:

- Fosc = 4 MHz
- T0CON = 0xC2
- INTCON = 0xA0

At what rate will the interrupt occur if the TMR0 is pre-loaded with the value 131? (15 marks)

Total 25 marks

END OF QUESTIONS

PLEASE TURN PAGE FOR PIC18F452 DATA SHEET

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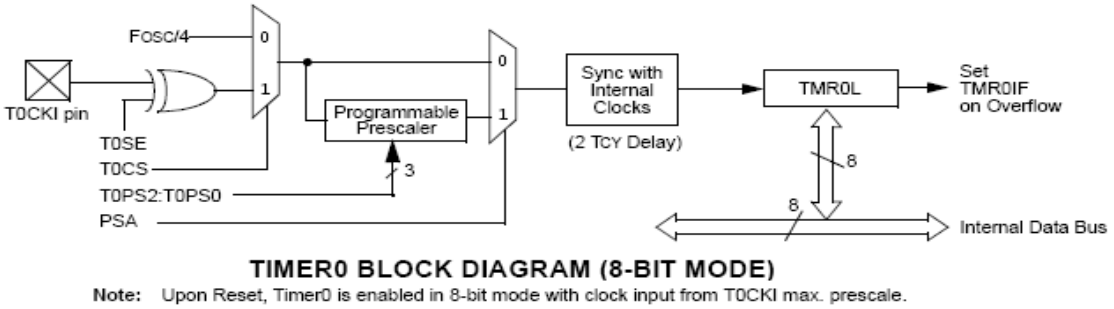
Data Sheet Information for the PIC18F452 Microcontroller



TIMER0 BLOCK DIAGRAM (8-BIT MODE)

Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Fig. 4: Timer0 Block Diagram.

T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

Fig. 5: Timer0 Control Register.

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INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Fig. 6: INTCON register.

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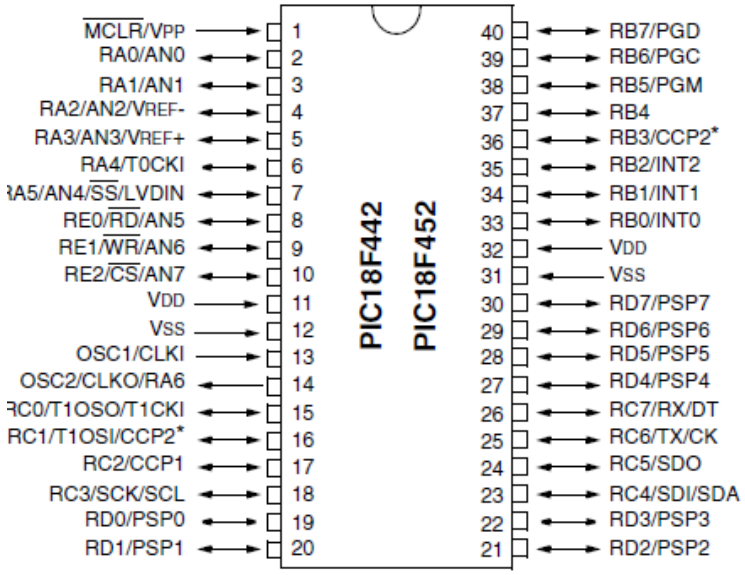

Fig. 7: PIC18F452 Pinout

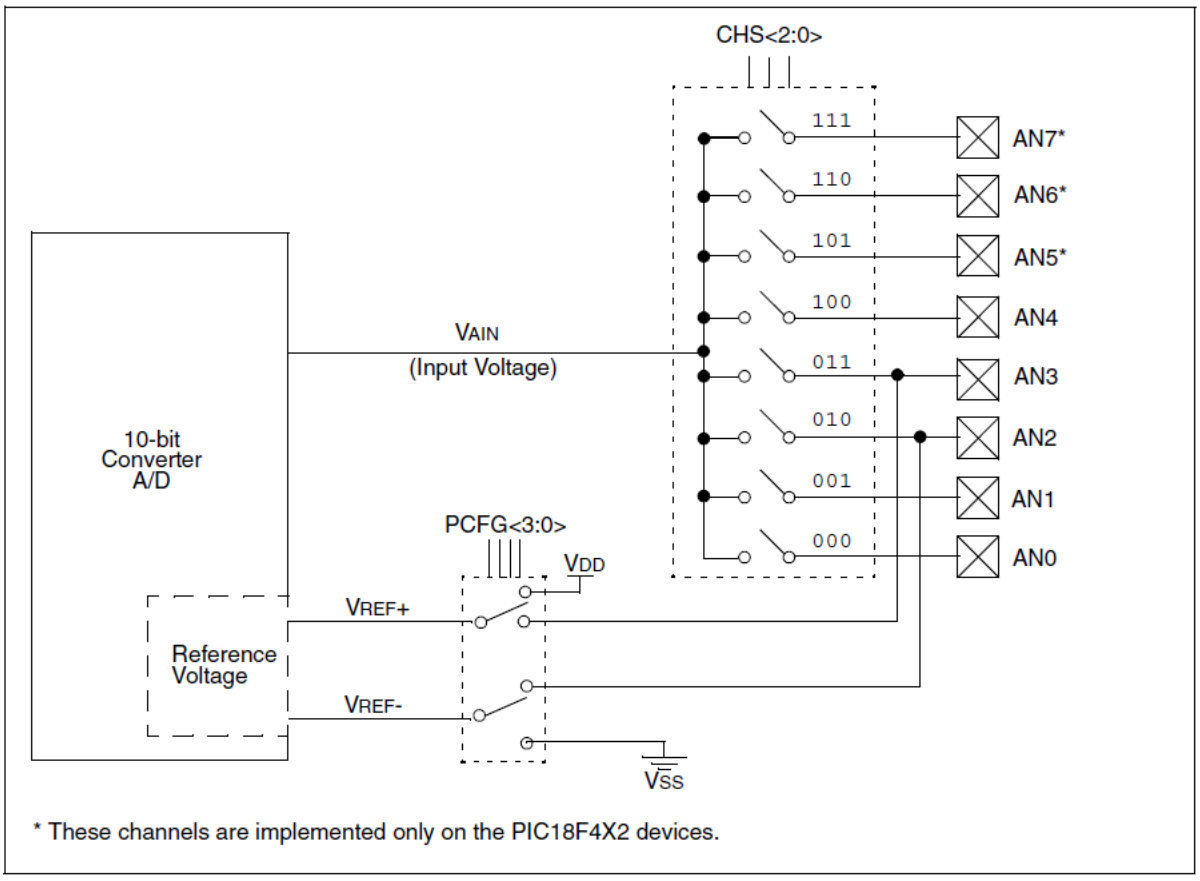

Fig. 8: ADC Block diagram.

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	FOSC/2
0	**01**	FOSC/8
0	**10**	FOSC/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	FOSC/4
1	**01**	FOSC/16
1	**10**	FOSC/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit
1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Fig. 9: ADCON0 Register.

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R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C / R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8 / 0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7 / 1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5 / 0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4 / 1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3 / 0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2 / 1
011x	D	D	D	D	D	D	D	D	—	—	0 / 0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6 / 2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6 / 0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5 / 1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4 / 2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3 / 2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2 / 2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1 / 0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1 / 2

A = Analog input D = Digital I/O
C/R = # of analog input channels / # of A/D voltage references

Fig. 10: ADCON1 Register.

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