UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER TWO EXAMINATION 2023/2024

ADVANCED EMBEDDED SYSTEMS

MODULE NO: EEE6017

Date: Thursday 16th May 2024 **Time: 10:00 – 12:30**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

Answer any FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

This assessment paper carries a total of 100 marks.

All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

CANDIDATES REQUIRE:

Extract from the PIC18F452 data sheets is provided at the back of the paper.

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Question 1

a) Fill in the missing entries, which are not shaded, in Table Q1a. Show all the steps that lead to the solution. State the suffix that is commonly used to represent hexadecimal number when writing software on MPLAB X?

Hexadecimal	Binary	Decimal
	10011011	**??**
	??	23
CF	**??**	**??**

Table Q1a

(9 marks)

b) PIC Microcontroller uses Harvard architecture. With the aid of a block diagram, explain Harvard architecture and list one advantage and one disadvantage for this architecture.

(16 marks)

Total 25 marks

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Question 2

a) A given memory chip has 12 address pins and 8 data pins, what is the memory organisation of this chip and the chip's capacity?

(6 marks)

b) What is the stack in a microcontroller? Explain how does the stack work with program counter during execution.

(8 marks)

c) Analyse and explain the following assembly code and illustrate the contents in the file register RAM location after each ADDWF command, in hexadecimal values.

```
MOVLW   0
MOVWF   15H
MOVLW   25H
ADDWF   15H, F
ADDWF   15H, F
ADDWF   15H, F.
```

(11 marks)

Total 25 marks

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Question 3

a) When the microcontroller powers up, it must start running its program from its beginning and explicit circuitry is built in to detect power-up and force the microcontroller to be initialised prior to the start of system operation. The below diagram (Figure 3a) presents a power-on reset circuit for the PIC18 microcontroller.

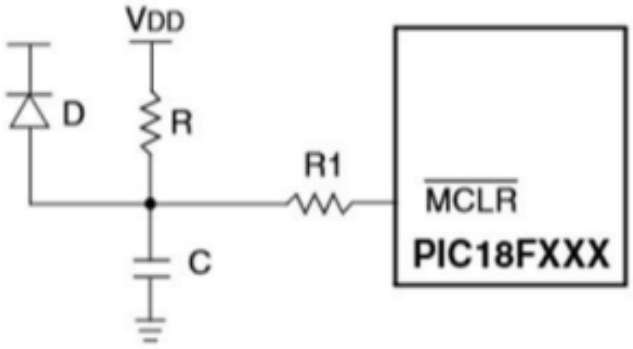

Figure 3a

Explain the function of each component and how this circuit ensures a power-on reset. (8 marks)

b) When working with a PIC microcontroller, you can select the oscillator mode in the configuration register to enable the microcontroller to operate in a timely manner. Your system requires a 12 MHz clock frequency, explain which oscillator mode will you choose to meet the requirement.

(5 marks)

c) Illustrate how a quartz crystal can be interfaced with a PIC microcontroller and discuss the advantages of using a quartz crystal. What are the recommended electronic component values to meet the clock frequency requirement given in Q3b?

(12 marks)

Total 25 marks

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Question 4

An embedded system uses a PIC microcontroller to drive a 12V DC motor that is connected via a transistor switch with a current gain (hfe) of 110. The system comprises of 1 red LED, 1 green LED and 2 buttons that are interface as stated below:

List Port	Connected Component to Port
Port B Pin 1	Button 1
Port B Pin 2	Button 2
Port B Pin 6	Green LED
Port B Pin 5	Red LED
Port B Pin 7	DC motor with a 100 ohms resistive load for the motor.

The buttons are connected as active high configuration and the LEDs are configured as active high mode. The LEDs require a forward current of 20mA, and have a forward voltage of 2.5V. The voltage between the emitter and the base, V_{be}, of the transistor is 0.7 V and the microcontroller is supplied with a 5V voltage.

Based on the above information, determine the following:

a) Draw the circuit diagram required for this design.

(6 marks)

b) Determine the values of any components that are required for the design.

(10 marks)

c) Write a 'C' code to show that when:
- Button 1 is pressed, motor is ON, green LED is ON and red LED is OFF.
- Button 2 is pressed, motor is OFF, green LED is OFF and red LED is ON.

(9 marks)

Total 25 marks

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Question 5

a) Provide the definition of the following common design metrics:
- Maintainability
- Time-to-prototype
- NRE Cost

(6 marks)

b) Explain what union is in relation to C programming and provide a coded example of how union data types is applied in a program.

(9 marks)

c) State the main advantage of using call by reference function and illustrate an example of a call by reference method.

(10 marks)

Total 25 marks

Question 6

a) Illustrate with the aid of a diagram a timer functional block diagram and what interrupt operation involves the RCON register?

(10 marks)

b) A PIC18F452 microcontroller, with a clock frequency of 16 MHz, is configured as a 8-bit timer to generate an interrupt on each timer count overflow. The pre-scaler is enabled on the TMR0 module and the pre-scale bits of 100 is applied. Determine, including all workings and considerations, the interrupt period that will be generated. Show how the Timer0 control register will be configured for this timer interrupt.

(15 marks)

Total 25 marks

END OF QUESTIONS

Please turn the page for data sheets.

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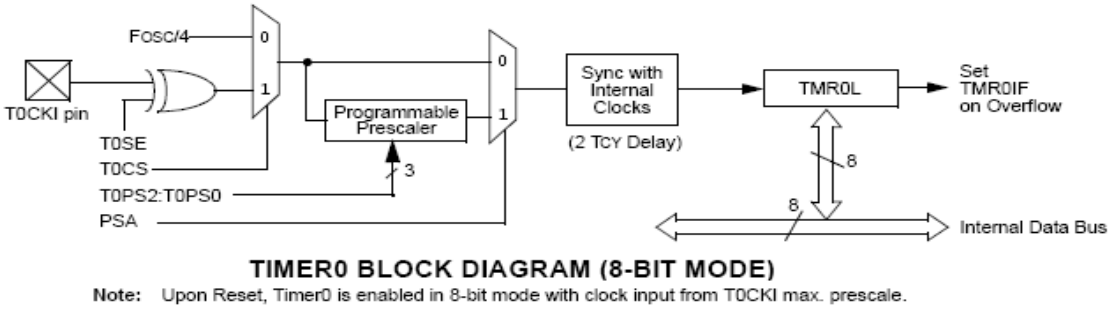
Data Sheet Information for the PIC18F452 Microcontroller



TIMER0 BLOCK DIAGRAM (8-BIT MODE)

Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Figure 1: Timer0 Block Diagram

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T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

Figure 2: Timer0 Control Register

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INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Figure 3: Interrupt Control register (INTCON)

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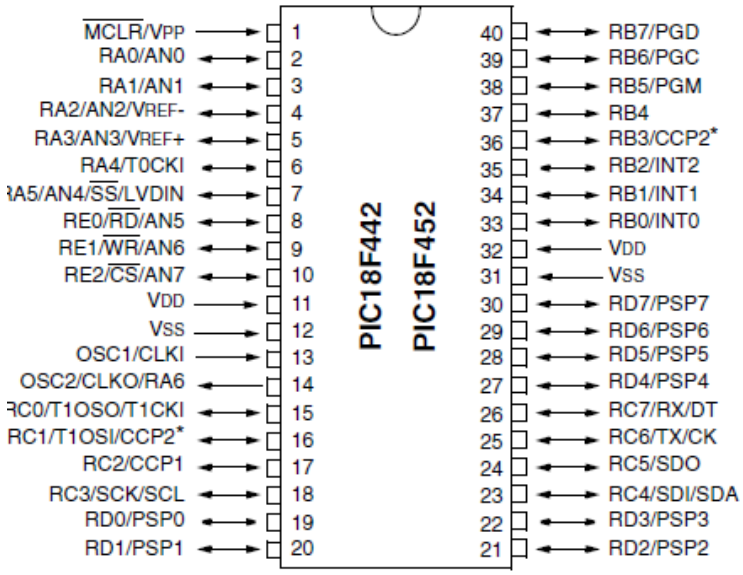

Figure 4: PIC18F452 Pinout

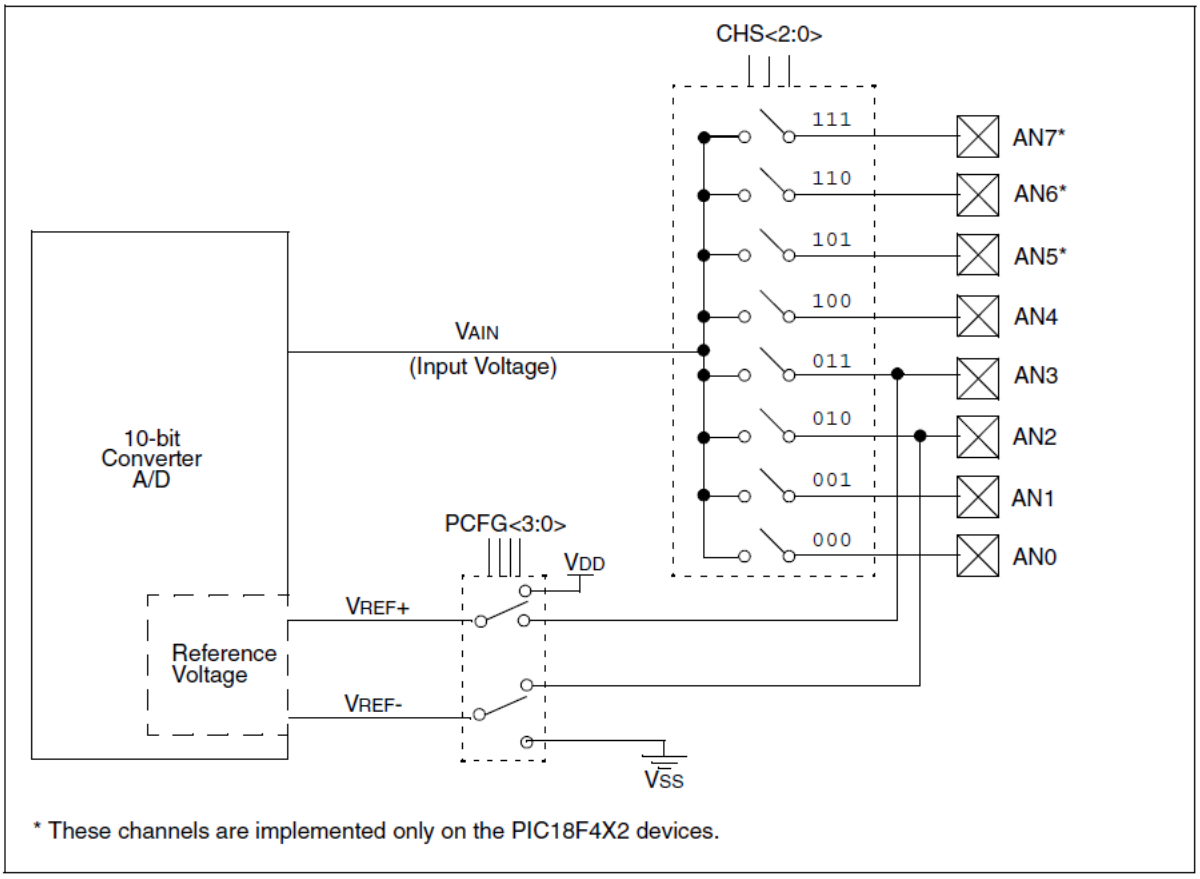

Figure 5: ADC Block diagram

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	FOSC/2
0	**01**	FOSC/8
0	**10**	FOSC/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	FOSC/4
1	**01**	FOSC/16
1	**10**	FOSC/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit
1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Figure 6: ADCON0 Register

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R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	FOSC/2
0	01	FOSC/8
0	10	FOSC/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	FOSC/4
1	01	FOSC/16
1	10	FOSC/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C / R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8 / 0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7 / 1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5 / 0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4 / 1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3 / 0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2 / 1
011x	D	D	D	D	D	D	D	D	—	—	0 / 0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6 / 2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6 / 0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5 / 1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4 / 2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3 / 2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2 / 2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1 / 0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1 / 2

A = Analog input D = Digital I/O
C/R = # of analog input channels / # of A/D voltage references

Figure 7: ADCON1 Register

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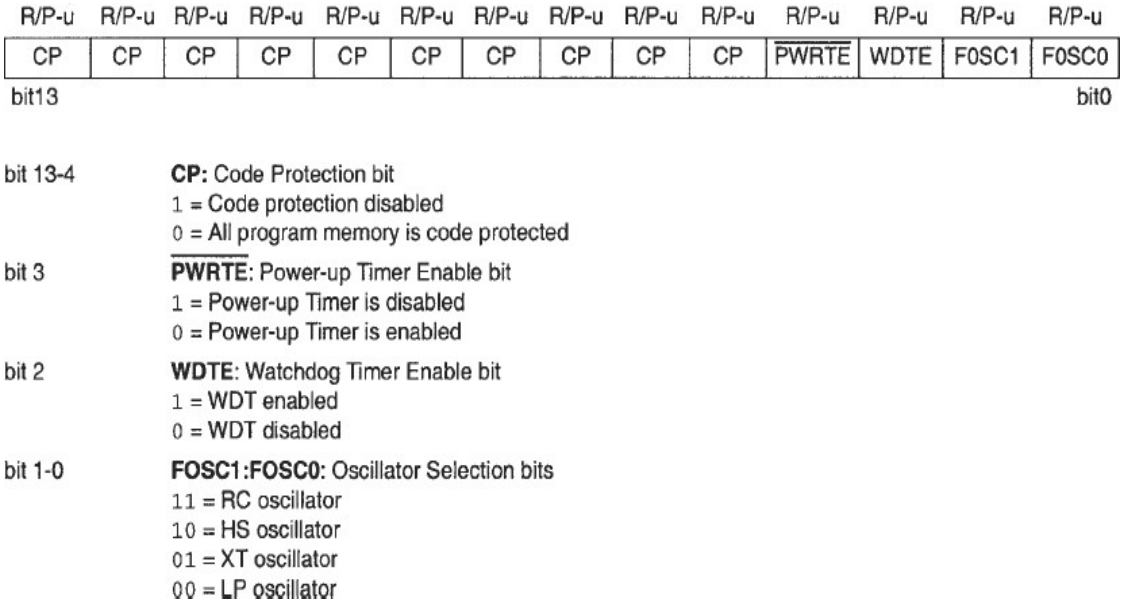

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	F0SC1	F0SC0
bit13													bit0

bit 13-4 **CP:** Code Protection bit
1 = Code protection disabled
0 = All program memory is code protected

bit 3 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = Power-up Timer is disabled
0 = Power-up Timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Figure 8: Configuration Register

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