UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER 2 EXAMINATIONS 2023/2024

INTRODUCTORY DIGITAL ELECTRONICS

MODULE NO: EEE4013

Date: Tuesday 14th May 2024 **Time:10:00 – 12:00**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.
Answer ANY FOUR questions.
All questions carry equal marks.
Marks for parts of questions are shown in brackets.
This examination paper carries a total of 100 marks.
All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

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Question 1

a) Complete the missing entries, **which are not shaded,** in the following table. Please show all the steps that lead to the solution. **[8 marks]**

Hexadecimal	Binary	Decimal
		26
	100001	
A2		
	1011100	

b) Solve the following and provide the answer in decimal (base-10).

1) 11100_2 x 10010_2 = _____$_{10}$
2) 10010_2 - 1110_2 = _____$_{10}$
3) 0101_{BCD} + 0011_{BCD} = _____$_{10}$
4) 1011_2 + 1100_2 = _____$_{10}$ **[12 marks]**

d) You are going to use a shaft encoder to track the current position of a rotatory motor, and the encoder implement Gray code rather than the Binary code. Explain the difference between the Gray code and Binary code, and what is the advantage of using Gray code? **[2 marks]**

e) Apply the rules of Boolean Algebra to simplify the following expression **[3 Marks]**

$$A.\overline{B}.C + B.C + A.\overline{C}$$

Total 25 marks

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Question 2

Consider the circuits shown in Figure Q2. The model in Q2 consists of 4 inputs.

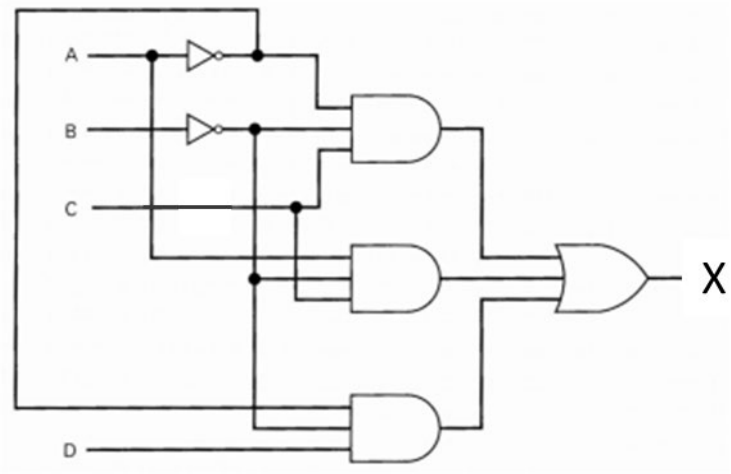

Figure Q2

a) Analyse the circuit and write the Boolean expression of the output X in the Figure Q2. **[5 marks]**

b) Determine the value of X for all the possible input conditions in Figure Q2 and list the values in a truth table. **[10 marks]**

c) You are an electrical engineer and you want to reduce the power consumption and cost in the above given circuit.

i) Based on the truth table obtained in Q2.b to create a Karnaugh map, reduce the logic functions into minimised SOP (sum-of-product) form.

[7 marks]

ii) Draw the new circuit diagram**.** **[3 marks]**

Total 25 Marks

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Question 3

a) Figure Q3.a1 is a 2-bit comparator with one output A=B. The timing waveform of 4 inputs are shown in Figure Q3.a2, please determine and draw the timing waveform below at the output (A=B). **[5 Marks]**

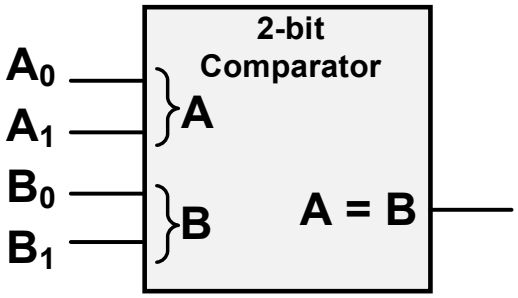

Figure Q3.a1: 2-bit Comparator

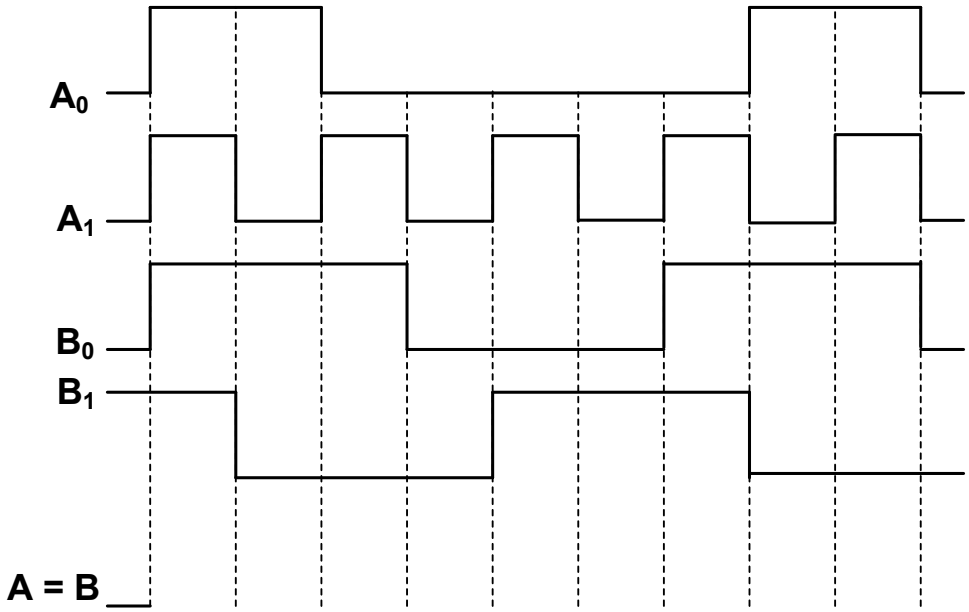

Figure Q3.a2: Comparator Timing Waveforms

Question 3 continues on next page

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Question 3 continues

b) Determine the sum generated by the 3-bit adder shown in Figure Q3.b below, as well as the carriers C1, C2 and C3 when binary numbers 100 and 110 are added. **[5 marks]**

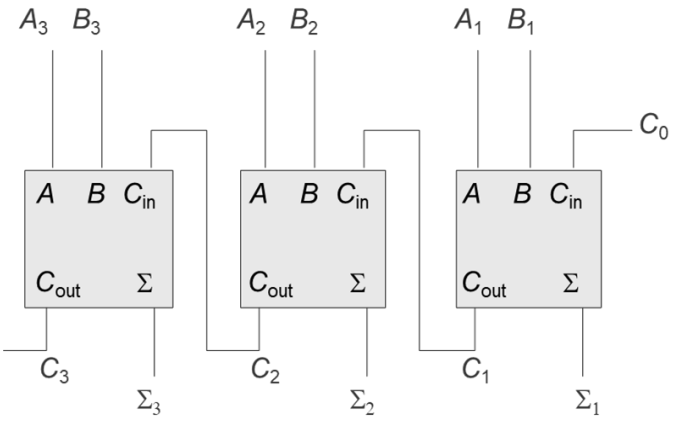

Figure Q3.b 3-bit adder

c) Figure Q3.c is a 4-bit shift-left register (uses D-flip-flops). Considering starting with setting Q3 Q2 Q1 Q0 outputs to 1011, and data input SI is steady logical 0,

i) decide what will be the new value after one active clock edge. **[3 Marks]**

ii) decide what will be the new value after 3 active clock edges**.** **[2 marks]**

iii) If the 4-bit register is a shift-right register, decide the new value after one active clock edge. **[2 Marks]**

Question 3 continues on next page

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Question 3 continues

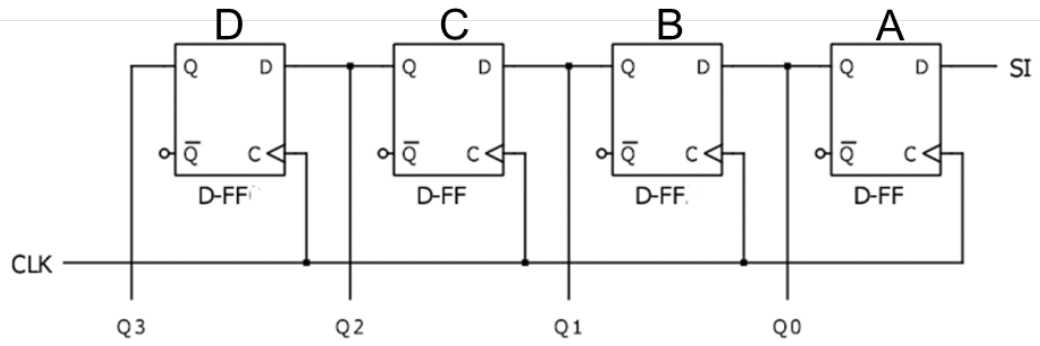

Figure Q3.c Diagram for 4-bit shift-left register

d) Explain the difference between a combinational logic circuit and a sequential circuit. Use system diagram to assist your explanation. **[8 marks]**

Total 25 Marks

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Question 4

SN74LS93 is a 4-bit ripple counter has a 40 MHz clock signal applied its CP_0' clock input pin.

a) What is the maximum possible modulus (MOD) number of this counter?

[5 marks]

b) What will be the frequency at the MSB output**?** **[5 marks]**

c) What is the duty cycle of the MSB output? **[3 marks]**

d) Assume that the counter starts at zero. What will be the count in decimal after 17 input pulses? **[4 marks]**

e) You need a 8-bit counter in your circuit design but you only have access to several SN74LS93 ICs at the moment. Explain what would you do to make the 8-bit counter. **[4 marks]**

f) Ripple counter is classified as asynchronous counter. Explain the difference between asynchronous counters and synchronous counters. **[4 marks]**

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Question 5

a) For the circuit shown below (Figure Q5.a1), the J-K inputs for both the flip-flops are tied to HIGH. The clock signal, fin, is shown in Figure Q5.a2.

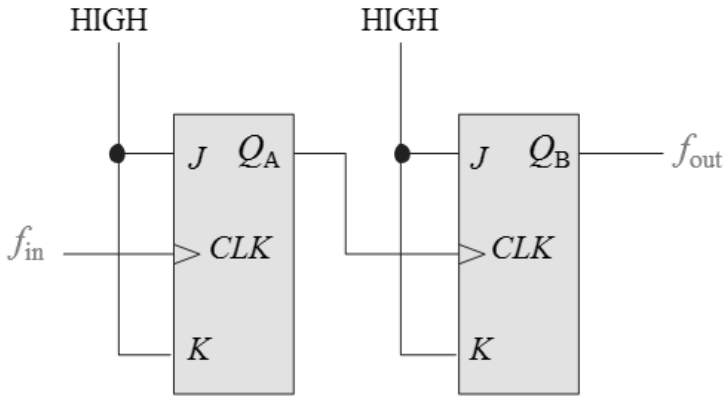

Figure Q5.a1 J-K flip-flops configured with both J and K inputs connected to HIGH

Figure Q5.a2 Input clock signal to the above J-K flip-flops

(i) With the help of appropriate waveforms, draw and describe the outputs from Q_A and Q_B (f_{out}). **[7 marks]**

(ii) If the input frequency (f_{in}) has a clock frequency of 25 MHz what will be values of the frequencies available at Q_A and Q_B? **[8 marks]**

Question 5 continues on next page

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Question 5 continues

b) Determine the output of a gated D latch for the inputs in Figure Q5.b?

[5 Marks]

Figure Q5.b: Gated D Latch Timing Waveform

c) Assuming the output of the Active HIGH decoder shown below (Fig. Q5.c) is a logic "1". Determine the inputs conditions needed, and write the logic expression of this decoder.

[5 marks]

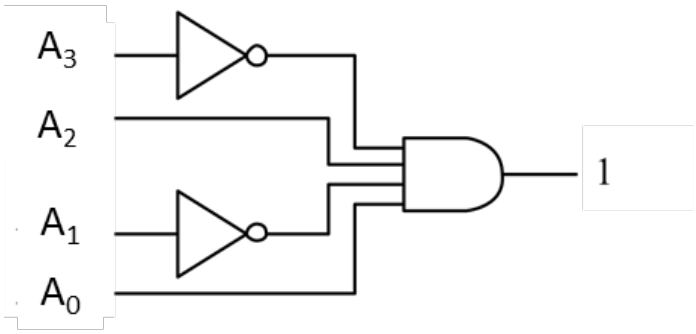

Figure. Q5.c Diagram of the decoder

Total 25 Marks

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Question 6

a) Draw the waveform of Q from a negative edge triggered J-K-flip flop **[5 Marks]**

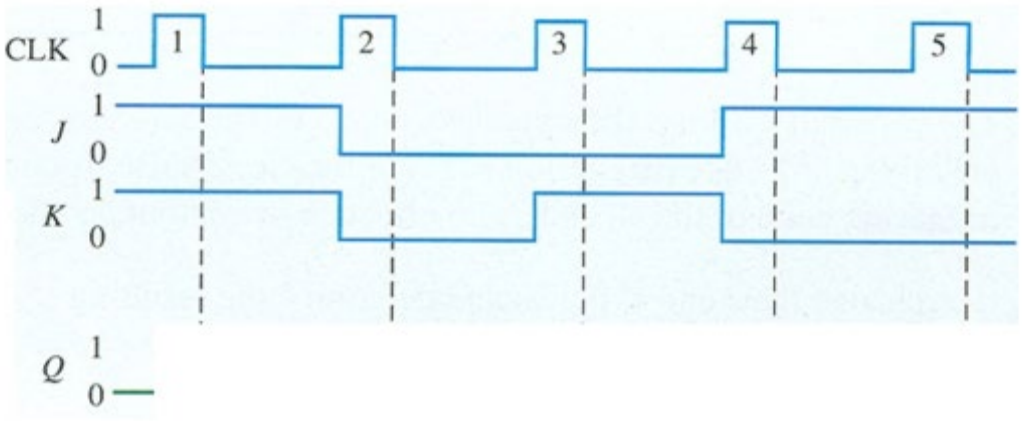

Figure Q6.a Input and clock waveform to the JK Flip Flop

b) For the circuit shown in Fig. Q6.b, construct a Truth Table for the logical functions at points C, D and Q. Then from the truth table obtained, identify a single logic gate that can be used to replace the complete circuit. **[12 marks]**

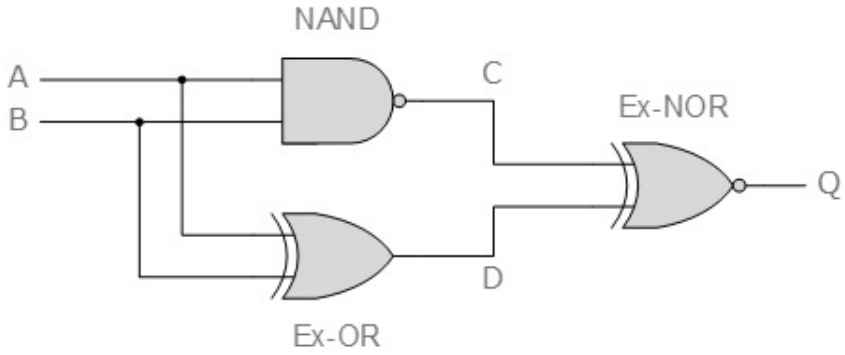

Figure 6.b circuit diagram

Question 6 continues on next page

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Question 6 continues

c) the device shown in Figure Q6.c is most likely a **[3 Marks]**

A. Comparator

B. Multiplexer

C. Demultiplexer

D. Encoder

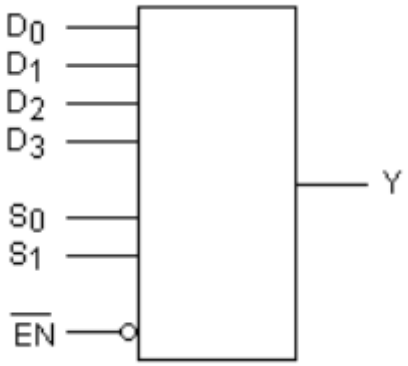

Figure Q6.c

d) For the device shown in Fig.Q6.2, if D0 = 1, D1 = 1, D2 = 0, D3 = 0, S0 = 1, S1 = 0, EN = 0, what is the status of the Y output? **[5 marks]**

Total 25 Marks

END OF QUESTIONS

END OF PAPER