ENG14

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL & ELECTRONIC ENGINEERING

SEMESTER 2 EXAMINATION - 2022/2023

INTERMEDIATE DIGITAL ELECTRONICS AND COMMUNICATIONS

MODULE NO: EEE5012

Date: Wednesday 10th May 2023 **Time: 10:00am – 12:30pm**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

You should answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

CANDIDATES REQUIRE:

None.

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Question 1

i. Using a fully illustrated diagram of a 4-bit full-adder circuit, design and determine how a digital electronic circuit compute.

a) 8 – 6

[10 marks]

b) 8 + 6

[10 marks]

Be sure to indicate the control signal (mode) bit, minuend bits, subtrahend bits and sum bits in each case.

ii. Write a code for 4 – Bit Full Adder using Behavioral Modelling.

[5 marks]

[Total 25 marks]

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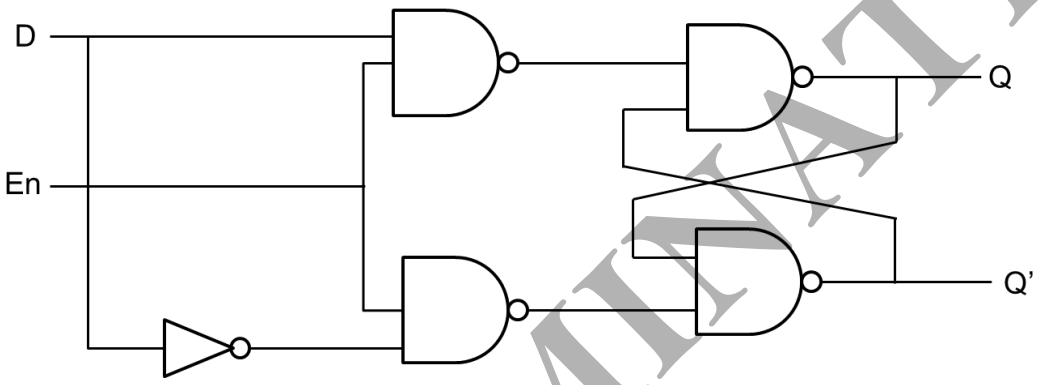
Question 2

The diagram below shows a D-Latch that is built using four NAND gates and an inverter.

i. Consider the following two other ways for obtaining a D latch. In each case draw the logic diagram and provide the equations to verify the circuit operation.



a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.

[5 Marks]

b) Use NOR gates for all four gates. Inverters maybe needed.

[5 Marks]

c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate in the above Fig. (that goes to the SR latch) to the input of the lower gate (instead of the inverter output).

[5 Marks]

ii. What is the main difference between an initial statement and an always statement in Verilog HDL?

[5 Marks]

iii. Explain the differences among a truth table, a state table, a characteristic table and an excitation table.

[5 Marks]

Total [25 Marks]

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Question 3

You are working as an electronic design engineer; due to supply shortages, only some specific flip-flop families are supplied, for example D flip-flops. However, you are required to design synchronous counters for mission critical applications in which J-K flip-flops must be used. Since flip flops can be converted from one form to another, you are required to convert the D flip-flops J-K flip-flops.

a) Using the excitation tables of J-K flip-flop and D flip-flop, determine the truth table for converting a D flip-flop to a J-K flip-flop.

[10 marks]

b) Using a suitable K-map, determine the suitable Boolean expression for converting D flip-flop to J-K flip flop.

[10 marks]

c) Draw the logic circuit diagram for converting D flip-flop to J-K flip flop, provide the characteristic equation of a J-K flip flop with justification.

[5 marks]

[Total 25 marks]

Question 4

You have been invited for an interview with a telecom provider but before you can be interviewed you receive some sample test questions. Through the knowledge you acquired during your studies

a) Identify and briefly explain any three types of modulation schemes.

[9 marks]

b) Explain why QAM does not involve changes in the frequency.

[5 mark]

c) Connect-X is an emerging telecommunications company. It has procured a certain frequency band from Ofcom and thinks of how to maximize it. You were recruited as their expert telecommunications engineer:

i. Identify what modulation scheme that would encourage high data rate

[6 marks]

ii. Explain with suitable diagram, the type of modulation scheme in 4c-i.

[5 marks]

[Total 25 marks]

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Question 5
Part - 1

A sequential circuit with two D flip flops A and B, two inputs x and y, and one output z is specified by the following next state and output equations:

$$A(t+1) = x'y + xB$$

$$B(t+1) = x'A + xB$$

$$z = A$$

a) Draw the logic diagram of the circuit.

[5 marks]

b) List the state table for the sequential circuit.

[5 marks]

c) Draw the corresponding state diagram.

[5 marks]

Part - 2

Figure below (page 6) show combinational and sequential circuits combined into one single system. At the positive rising edge of the clock (CLK) input, the system gives outputs A, B and Y given the X input. Determine the

d) state equation of the system

[5 Marks]

e) excitation table.

[5 Marks]

Question 5 continues over the page

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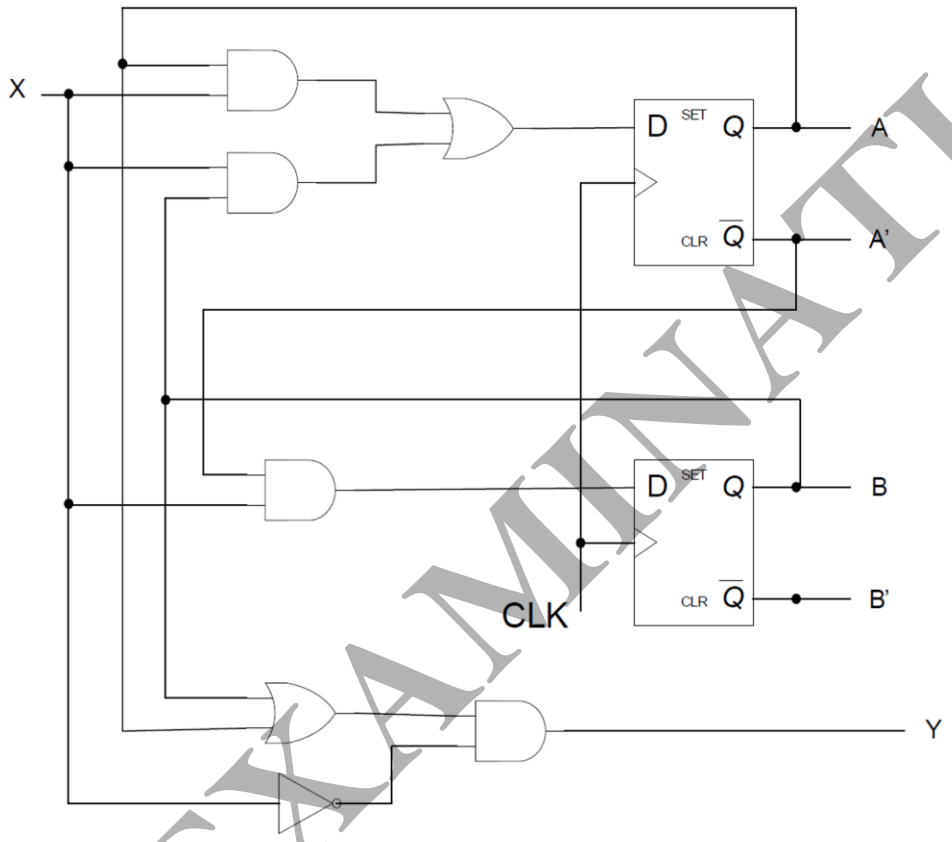
Question 5 continued



Sequential logic circuit and combinational logic circuit

Total [25 Marks]

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Question 6: Explain the following.

a) What are three programming techniques that can be used in Verilog, and how do they differ in their approach to hardware design?

[10 Marks]

b) State the difference between wire and reg data types?

[5 Marks]

c) State the difference between initial and always procedural blocks?

[5 Marks]

d) Write the Verilog code for a 4-bit comparator using behavioral modeling.

[5 Marks]
Total [25 Marks]

END OF QUESTIONS.