UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER TWO EXAMINATION 2022/2023

INTRODUCTORY DIGITAL ELECTRONICS

MODULE NO: EEE4013

Date: Tuesday 9th May 2023   Time: 10:00 – 12:00

INSTRUCTIONS TO CANDIDATES: There are **SIX** questions.

Answer **ANY FOUR** questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

This examination paper carries a total of 100 marks.

All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

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Question 1

a) What is the difference between the Gray code and Binary code? Provide an example of where the Gray code can be used. **[2 marks]**

b) Show how the binary code, 1100110, can be converted to its equivalent Gray code. **[3 marks]**

c) Perform the following arithmetic operations. Please note carefully the radix (base) of the number system:

(i) $2A_{16} + 6B_{16} = XX_{10}$ **[5 marks]**

(ii) $1101_2 \times 1101_2 = XX_{10}$ **[5 marks]**

d) Complete the missing entries, **which are not shaded,** in the following table. Please show all the steps that lead to the solution.

Hexadecimal	Binary	Decimal
	11010	
		33
		105
A2		

[10 marks]

Total 25 marks

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Question 2

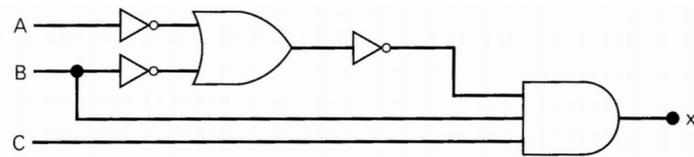Consider the circuits shown in Figure Q2. The model in Q2 consists of 3 inputs.

Fig.Q2

a) Write the Boolean expression of the output x in the Figure Q2.   **[5 marks]**

b) Determine the value of x for all the possible input conditions in Figure Q2, and list the values in a truth table.

[7 marks]

c) Using a Karnaugh map, convert the following expressions to a minimised SOP
(sum-of-product) form:

(i) $X = \overline{A}\,\overline{B}\,\overline{C} + \overline{AB}CD + A\overline{C}\,\overline{D} + \overline{A}CD + A\overline{B}C\overline{D}$ **[7 marks]**

(ii) $X = \overline{A}\,\overline{B} + A\overline{B}\,\overline{C} + A\overline{B}C + ABC$ **[6 marks]**

Total 25 Marks

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Question 3

(a) Determine the sum generated by the 4-bit parallel adder shown in Fig.Q3a below and show the intermediate carriers when binary numbers 1011 and 0011 are added.
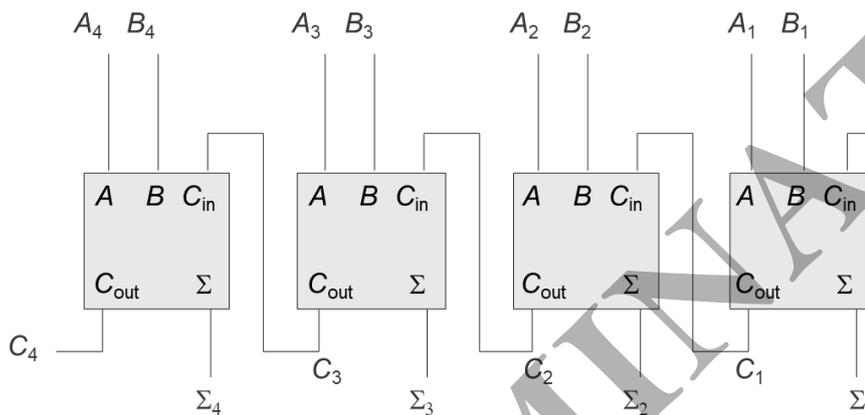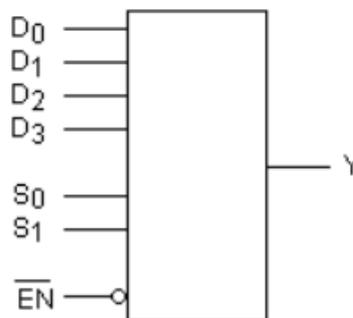

Fig. Q3a   **[5 marks]**

(b) the device shown in Fig.Q3b is most likely a   **[2 Marks]**

    A.   Comparator

    B.   Multiplexer

    C.   Demultiplexer

    D.   Encoder

Fig. Q3b

Question 3 continues over the page…

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…Question 3 continued

(c) For the device shown in Fig.Q3b, if D0 = 1, D1 = 1, D2 = 0, D3 = 0, S0 = 0, S1 = 1, EN = 0, what is the status of the Y output?   **[3 marks]**

(d) Baking parameter monitoring has become a standard practice in Bakery. A simple temperature alarm system for the oven can be realised by a comparator circuit and will alert the baker when the temperature exceeds a certain threshold (T_{ref})

   (i) What is a comparator?   **[2 marks]**

   (ii) Describe the working operation of temp monitoring to produce an alarm. What kind of comparator should be used for such an alarm system?**[6 marks]**

   (iii) Use a suitable diagram and truth table to determine the logic equation that demonstrates the output that will trigger the alarm.   **[7 marks]**
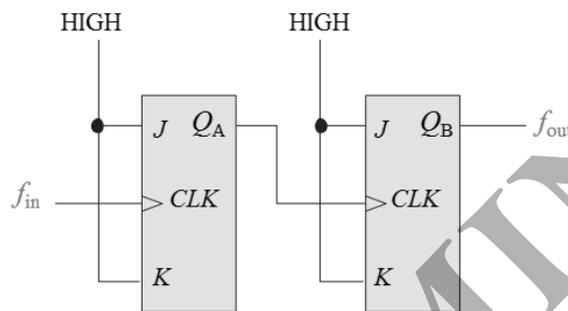
Total 25 Marks

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Question 4

a)   For the circuit shown below (Fig. Q4a), the J-K inputs for both the flip-flops are tied to HIGH.
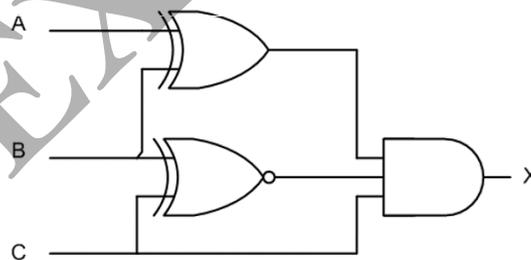
(i) With the help of appropriate waveforms, draw and describe the outputs from Q_A and Q_B (f_{out}).   **[7 marks]**

(ii) If the input frequency (f_{in}) has a clock frequency of 50 MHz what will be values of the frequencies available at Q_A and Q_B?   **[8 marks]**

Fig. Q4a

b)   Determine the input conditions needed to produce x= 1 for the circuit

below (Fig.Q4b):   **[5 marks]**

Fig. Q4b

Question 4 continues over the page…

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…Question 4 continued

c) Assuming the output of the decoder shown below (Fig. Q4c) is a logic "1". What

are the inputs to the Active HIGH decoder and the logic expression of the decoder?
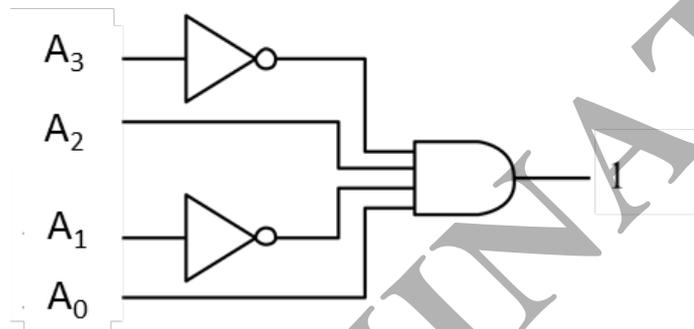
[5 marks]

Fig. Q4c

Total 25 Marks

Question 5

a) A 10-bit ripple counter has a 10 ns propagation delay for each of the edge-triggered flip flops. What can be the maximum clock frequency of this ripple counter which will not cause a count to skip? **[8 Marks]**

b) If this 10-bit ripple counter has a 512-kHz clock signal applied.

(i) What is the MOD number of this counter? **[5 marks]**
(ii) What will be the frequency at the MSB output? **[3 marks]**
(iii) What will be the duty cycle of the MSB signal? **[2 marks]**

(iv) Assume that the counter starts at zero. What will be the
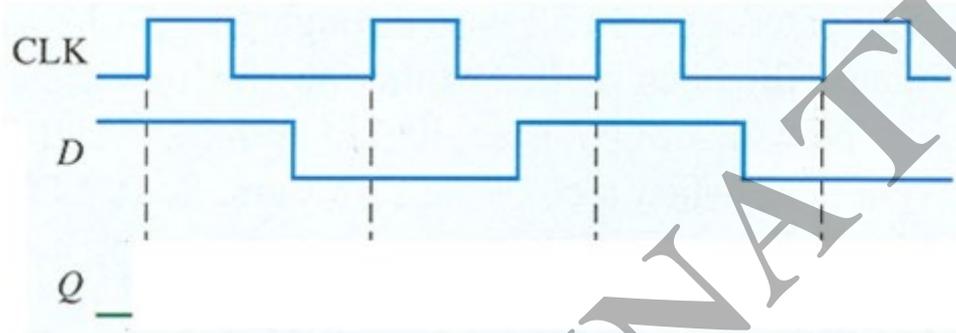count in hexadecimal after 1000 input pulses?

[7 marks]

Total 25 Marks

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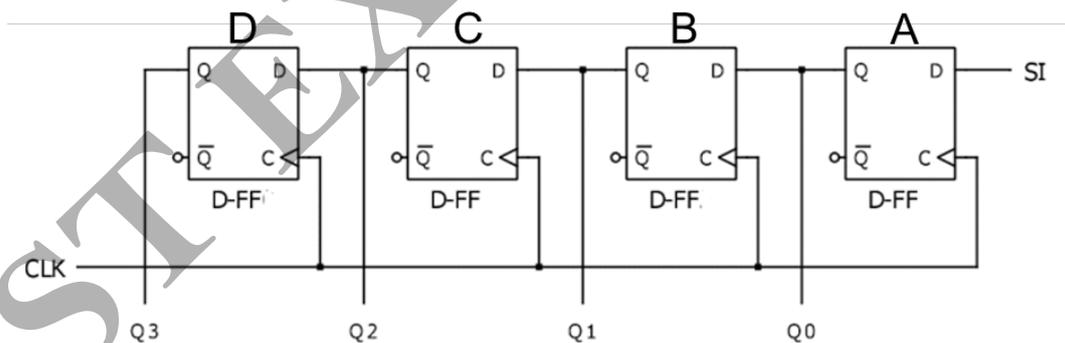Introductory Digital Electronics
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Question 6

a) Sketch and explain the difference between combinational logic circuit and sequential logic circuit. **[6 Marks]**

b) Draw the waveform of Q from a positive edge triggered D-flip flop **[6 Marks]**

Fig.Q6b

c) Fig.Q6c is a 4-bit shift-left register (uses D-flip-flops). Considering starting with seting Q3 Q2 Q1 Q0 outputs to 0110, and data input SI is steady logical 0, decide what will be the new value after one active clock edge. **[5 Marks]**

Fig.6Qc

Question 6 continues over the page…

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…Question 6 continued

d) For the same 4-bit shift-left register shown in Fig.Q6c, the operation starts with resetting all Q-outputs to logical 1, and the data input SI alternates between 0 and 1. Fill the table below to show the data in each stage after each of the four shift pulses and explain the operation.

[8 Marks]

Table Operation of shift-left register			
Shift Pulse	D	C	B	A
0	1	1	1	1
1				
2				
3				
4				

Total 25 Marks

END OF PAPER