[ENG29]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

MSC SYSTEMS ENGINEERING AND ENGINEERING MANAGEMENT

SEMESTER TWO EXAMINATION 2021/2022

MICROPROCESSOR BASED SYSTEMS

MODULE NO: EEM7016

Date: Thursday 19th May 2022 **Time: 10:00 – 12:00**

INSTRUCTIONS TO CANDIDATES: **There are SIX questions.**

Answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

This assessment paper carries a total of 100 marks.

All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

CANDIDATES REQUIRE: **Extracts from the PIC18F452 data sheets is provided at the back of the paper.**

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Question 1

a) Provide definition for the following design metric terms:
- NRE Cost
- Unit Cost
- Time-to-prototype

(6 marks)

b) Convert the decimal number 234 to a 8-bits binary number and also show it in hexadecimal value.

(4 marks)

c) What does the abbreviation ICD means?

(2 marks)

d) Illustrate in a diagram the Harvard architecture and list what are the advantages and disadvantages of this architecture.

(13 marks)

Total 25 marks

Question 2

a) Show in a diagram the architecture of a General Purpose Microprocessor System. Explain what is volatile memory.

(12 marks)

b) Explain and illustrate with the aid of a diagram what is structure diagram in software engineering.

(13 marks)

Total 25 marks

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Question 3

a) Determine the number of data and address pins for the EEPROM chip 28C256-15, as shown in Table Q3.

EEPROMs

Part No.	Capacity	Org.	Speed	Pins	V_{PP}
2816A-25	16K	2Kx8	250 ns	24	5 V
2864A	64K	8Kx8	250 ns	28	5 V
28C64A-25	64K	8Kx8	250 ns	28	5 V CMOS
28C256-15	256K	32Kx8	150 ns	28	5 V
28C256-25	256K	32Kx8	250 ns	28	5 V CMOS

Table Q3: EEPROM Memory Organisation

(5 marks)

b) Depict in a diagram showing a simplified PIC Microcontroller Architecture. What is the total number of instructions in a PIC18 microcontroller.

(20 marks)

Total 25 marks

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Question 4

A PIC microcontroller embedded system is connected to three buttons and three LEDS. The components connects to the following PIC microcontroller pins:

Button 1	PORTB 0
Button 2	PORTB 1
Button 3	PORTB 2
LED 1	PORTB 5
LED 2	PORTB 6
LED 3	PORTB 7

The buttons and LEDs are connected as active high mode to the microcontroller. Take into consideration that the LEDs require a forward current of 22mA, and have a forward voltage of 2.1V. The microcontroller is supplied by a 5V voltage.

Based on the above information provided, determine the following:

a) Draw the circuit diagram required for this design.

(6 marks)

b) Determine the values of any components that are required for the design.

(5 marks)

c) Write a 'C' function code showing how to initialise the port used in the system.

(4 marks)

d) Write a 'C' code to show that when:
   - Button 1 is pressed, LED 1 is ON and LED 2 and LED 3 is OFF.
   - Button 2 is pressed, LED 2 is ON and LED 1 and LED 3 is OFF.
   - Button 3 is pressed, LED 3 is ON and LED 1 and LED 2 is OFF.

(10 marks)

Total 25 marks

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Question 5

a) Define what does the term expression means in C programming and provide an example?

(4 marks)

b) Provide a simple C programming example of a switch case decision statement and also depict it in a flow chart.

(8 marks)

c) Illustrate in a diagram how a 4x4 matrix keypad can be connected to a PIC18F452 microcontroller. Identify and provide reasons on which microcontroller port the matrix keypad should be connected to.

(13 marks)

Total 25 marks

Question 6

a) The PIC18F452 consists of a 16-bit timer but the data bus is only 8-bits wide. Explain how a 16-bit timer read function is performed.

(6 marks)

b) What is the main difference in setting up the timer module as count or timer mode.

(4 marks)

c) In an industrial application, using a PIC18F452, Timer 0 is used to create a timed event using a timer interrupt. Determine the rate at which the interrupt will occur, based on the following timer module configurations for the microcontroller:

- F_{osc} = 1.6 MHz
- T0CON = 0xC3;
- INTCON = 0xA0;
- The timer module is pre-loaded with the count value of 6.

(15 marks)

Total 25 marks

END OF QUESTIONS

Data sheet information for the PIC18F452 Microcontroller over the page….

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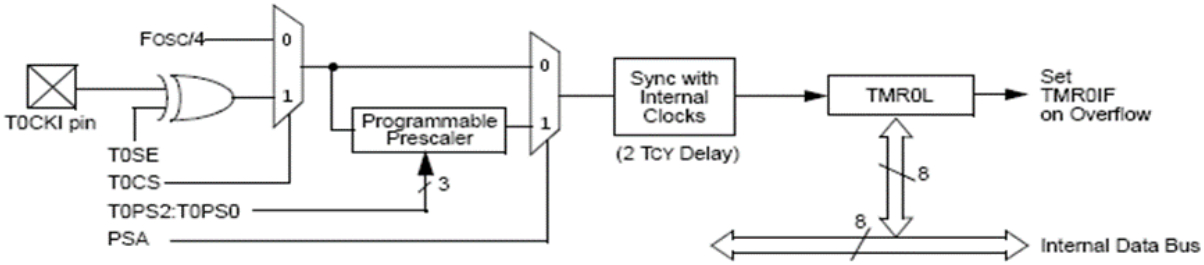
Data Sheet Information for the PIC18F452 Microcontroller



TIMER0 BLOCK DIAGRAM (8-BIT MODE)

Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Figure 1: Timer0 Block Diagram

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T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

Figure 2: Timer0 Control Register

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INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Figure 3: INTCON register

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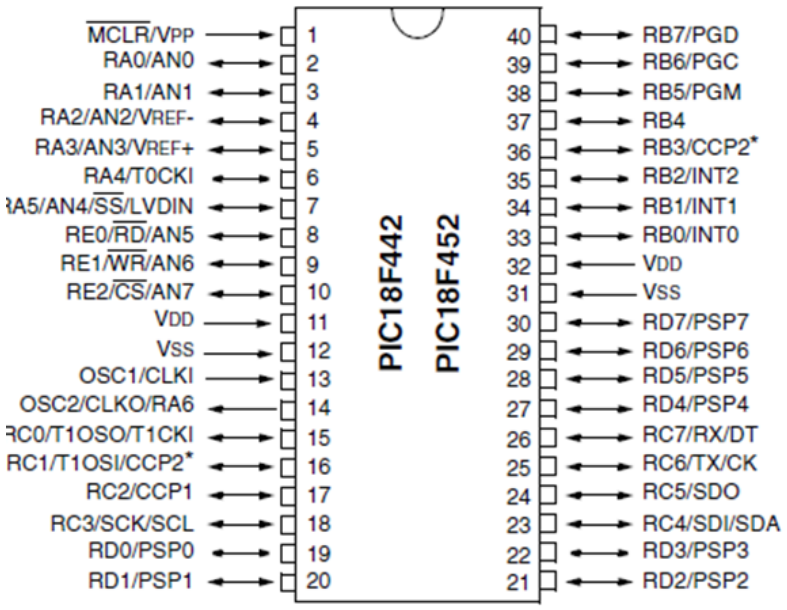

Figure 4: PIC18F452 Pinout

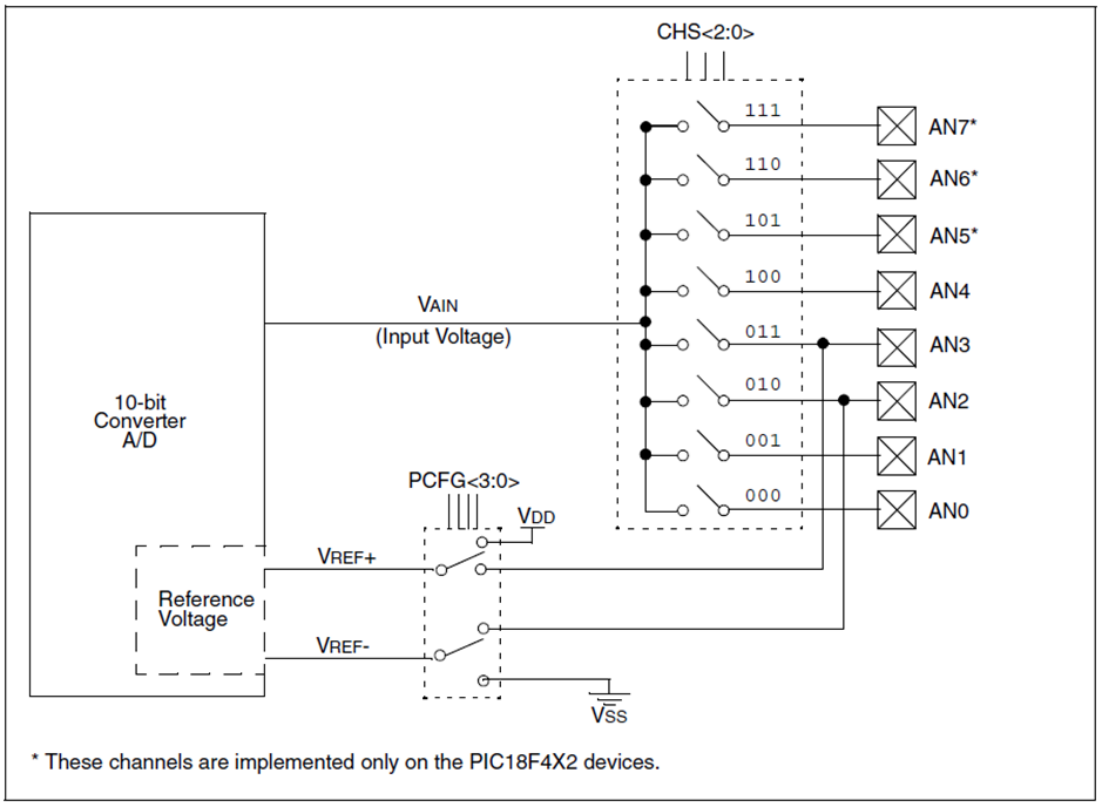

Figure 5: ADC Block diagram

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	Fosc/2
0	**01**	Fosc/8
0	**10**	Fosc/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	Fosc/4
1	**01**	Fosc/16
1	**10**	Fosc/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit
1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Figure 6: ADCON0 Register

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R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C / R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8 / 0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7 / 1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5 / 0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4 / 1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3 / 0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2 / 1
011x	D	D	D	D	D	D	D	D	—	—	0 / 0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6 / 2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6 / 0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5 / 1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4 / 2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3 / 2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2 / 2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1 / 0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1 / 2

A = Analog input D = Digital I/O
C/R = # of analog input channels / # of A/D voltage references

Figure 7: ADCON1 Register

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