[ENG36]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL & ELECTRONICS ENGINEERING

SEMESTER TWO EXAMINATIONS 2021/2022

INTERMEDIATE DIGITAL ELECTRONICS AND COMMUNICATIONS

MODULE NO: EEE5012

Date: Wednesday 18th May 2022 **Time: 10:00 – 12:30**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

You should answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Electronic calculators may be used provided that data and program storage memory is cleared prior to the In-Class Assessment.

CANDIDATES REQUIRE:

Calculator.

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Question 1

a) Overflow is an important factor to be considered when designing digital electronic systems. Using a suitable example, describe what is meant by an overflow. **[6 marks]**

b) Using a suitably labelled diagram, describe how overflow can be detected in a digital electronic circuit. **[13 marks]**

c) Describe how an overflow can be detected in signed numbers. **[6 marks]**

Total 25 marks

Question 2

To develop a finite state machine, some parts of the circuit require a sequential circuit and need to be analysed. Consider the following sequential circuit as shown in Figure Q2.

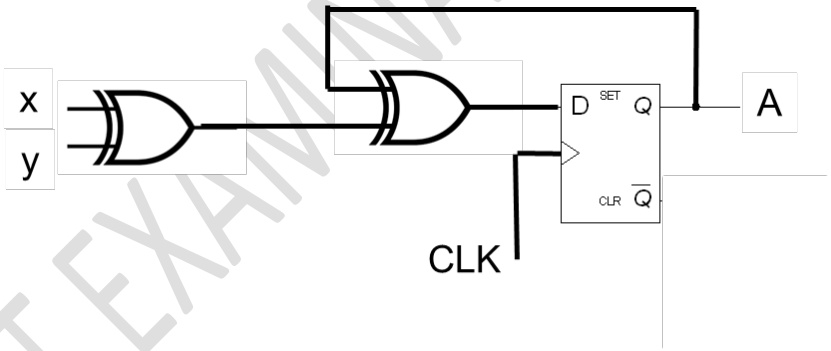

Figure Q2

a) Derive the excitation equations of the sequential devices. **[3 marks]**
b) Determine the state equations of system. **[3 marks]**
c) Determine and complete the state transition table. **[9 marks]**
d) Using the state transition table, draw the state diagram of the system. **[10 marks]**

Total 25 marks

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Question 3

a) Using suitable diagrams, describe the difference between Amplitude Phase Shift Keying and Frequency Shift Keying. **[14 marks]**
b) Describe what is meant by interleaving in time division multiplexing and explain why it is important. **[11 marks]**

Total 25 marks

Question 4

You have been employed by British Telecom as a Telecommunication Graduate Engineer. The company has won a new project to design and implement home telephone lines that would serve a newly built Dominion Village. The company is considering implementing voice communication to all homes in the Dominion Village using Frequency Division Multiplexing.

a) What is frequency division multiplexing? **[6 marks]**
b) If five channels, each with a 100-kHz bandwidth, are to be multiplexed together. What is the minimum bandwidth of the link if there is a need for a guard band of 10 kHz between the channels to prevent interference? **[6 marks]**
c) Draw a suitable diagram, with suitable labelling, showing the implementation in Question 4 – b). **[6 marks]**
d) Assume that a voice channel occupies a bandwidth of 4 kHz. We need to combine three voice channels into a link with a bandwidth of 12 kHz, from 20 to 32 kHz. Show the configuration using the frequency domain without the use of guard bands. **[7 marks]**

Total 25 marks

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Question 5

BAES is a UK-based defence company that uses electronic systems to design military equipment. As an electronic design engineer, you are to develop a logic digital electronic circuit for a system that would display the digits 0 – 9 decimals, ***as BCD***. Flip-flops that usually hold one-bit "0" or "1" will be used in the design. The clock and other inputs to the flip-flops are expected to be controlled externally.

a) What are BCDs ? **[4 Marks]**
b) Explain why they may be preferred in this design. **[2 Marks]**
c) Determine the number of flip-flops that are required. **[3 Marks]**
d) Design an electronic logic circuit to display **52** and **99**, ***as BCD***. **[16 Marks]**

Total 25 Marks

Question 6

You have been employed by the BMW car manufacturing company as a digital electronic engineer. Among the functionalities to be included in their new car design is a digital clock. The design considers the digital clock as a finite state machine. If the digital clock transitions from 0000 to 1011.

a) Using a suitably labelled schematic diagram, describe a typical digital electronic circuit that implements the digital clock showing how the clock returns to 0000 if the 12 states are exceeded. **[17 marks]**

b) Draw and label the state transition diagram showing how the clock works. **[6 marks]**
c) Explain why a digital clock that transits over 12 states does not require a high precision binary code system. **[2 marks]**

Total 25 Marks

END OF PAPER