[ENG 09]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER TWO EXAMINATIONS 2021/2022

ADVANCED EMBEDDED SYSTEMS

MODULE NO: EEE6017

Date: Thursday 19th May 2022 **Time: 10:00 – 12:30**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

Answer any FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

This assessment paper carries a total of 100 marks.

All working must be shown. A numerical solution to a question obtained by programming an electronic calculator will not be accepted.

CANDIDATES REQUIRE:

Extracts from the PIC18F452 data sheets is provided at the back of the paper.

School of Engineering
BEng (Hons) Electrical and Electronic Engineering
Semester Two Examinations 2021/2022
Advanced Embedded Systems
Module No. EEE6017

Question 1

a) Provide the definition of the following listed design metrics:
- Flexibility
- Time-to-market
- Maintainability

(6 marks)

b) What is the suffix that is commonly used to represent binary and hexadecimal number when writing software on MPLAB X? Show how the decimal number 140 will be presented in binary and hexadecimal number format in MPLAB X.

(6 marks)

c) Illustrate with the aid of a diagram showing a general purpose microprocessor system and specify what the term nibble is.

(13 marks)

Total 25 marks

Question 2

a) A memory chip has a capacity of 1024K and consists of 8 data pins, determine what is the memory organisation and the number of address pins for this chip.

(6 marks)

b) Explain and illustrate with the aid of a diagram the von-neumann architecture.

(15 marks)

c) How many one-word (16-bit) and two-words (32-bit) instructions can be found in the instruction set for a PIC18F452 microcontroller?

(4 marks)

Total 25 marks

Please turn the page...

Question 3

a) Design a state machine diagram, illustrating how a simple automated train ticket machine functions. Take into consideration the following requirements:
   - Only 1 person can buy a train journey ticket each time.
   - Each journey cost £5.00 and exact change is not needed.
   - The machine is able to refund the user's money at any time.
   - Only the following currencies are accepted:
     - Coins: £1, £2
     - Note: £5 and £10.

(15 marks)

b) Which oscillator modes can be operated with the ceramic resonator?

(4 marks)

c) How can the micro-controller wake up from sleep mode?

(6 marks)

Total 25 marks

Question 4

a) What are the stages that is involved in building a C program and state text substitution occurs at which stage.

(10 marks)

b) Write a C programming example of a forever loop.

(5 marks)

c) Design a simple C program that uses structures and typedef, include how this functions with the main part of the program.

(10 marks)

Total 25 marks

Please turn the page…

Question 5

An embedded system uses a PIC microcontroller to interface to three buttons and three LEDS. The components connects to the following PIC microcontroller pins:

Button 1	PORTB 0
Button 2	PORTB 1

Button 3	PORTB 2
LED 1	PORTB 4
LED 2	PORTB 5
LED 3	PORTB 6

The buttons and LEDs are connected as active high mode to the microcontroller. The LEDs require a forward current of 22mA, and have a forward voltage of 2.1V. The microcontroller is supplied by a 5V voltage.

Based on the above information, determine the following:

a) Draw the circuit diagram required for this design.

(6 marks)

b) Determine the values of any components that are required for the design.

(5 marks)

c) Write a 'C' function code showing how to initialise the system.

(4 marks)

d) Write a 'C' code to show that when:
- Button 1 is pressed, LED 1 is ON and LED 2 and LED 3 is OFF.
- Button 2 is pressed, LED 1 and LED 2 is ON, LED 3 is OFF.
- Button 3 is pressed, LED 1, LED 2 and LED 3 are ON.

(10 marks)

Total 25 marks

Please turn the page over.

Question 6

a) List two types of interrupts that is supported by the PIC microcontroller.

(4 marks)

b) In an industrial application, using a PIC18F452, a packaging machine counts boxes and packages in packs of 100 boxes. Whenever a box passes by a sensor connected to the RA4/T0CK1 pin of the microcontroller, the sensor will produce a High logic pulse.

(i) Explain how the Timer0 module will be configured to count the boxes applying the polling method. The block diagram of the Timer0 module can be found in Figure 1 of the datasheet information provided.

(5 marks)

(ii) Elaborate in details how using an interrupt, using pseudocode examples, can allow the microcontroller program to detect the 100th box that was counted, which then reset the machine to enable it to count and package the next batches of 100 boxes.

(16 marks)

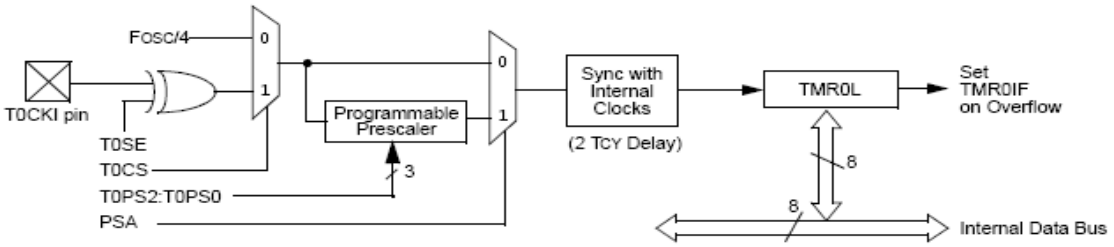
Total 25 marks

END OF QUESTIONS

Data Sheet Extracts follow on the next pages

Please turn the page…

Data Sheet Information for the PIC18F452 Microcontroller



TIMER0 BLOCK DIAGRAM (8-BIT MODE)

Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Figure 1: Timer0 Block Diagram

T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

Figure 2: Timer0 Control Register

Please turn the page…

INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 **GIE/GIEH:** Global Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit

1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Figure 3: Interrupt Control register (INTCON)

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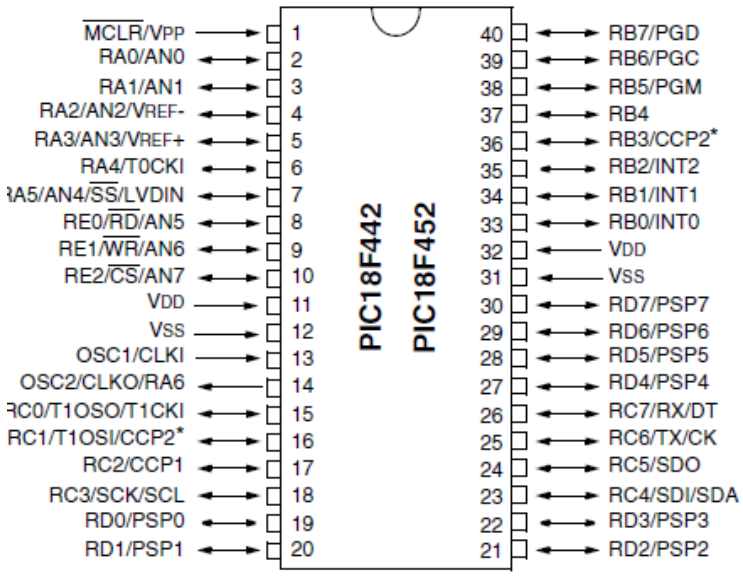

Figure 4: PIC18F452 Pinout

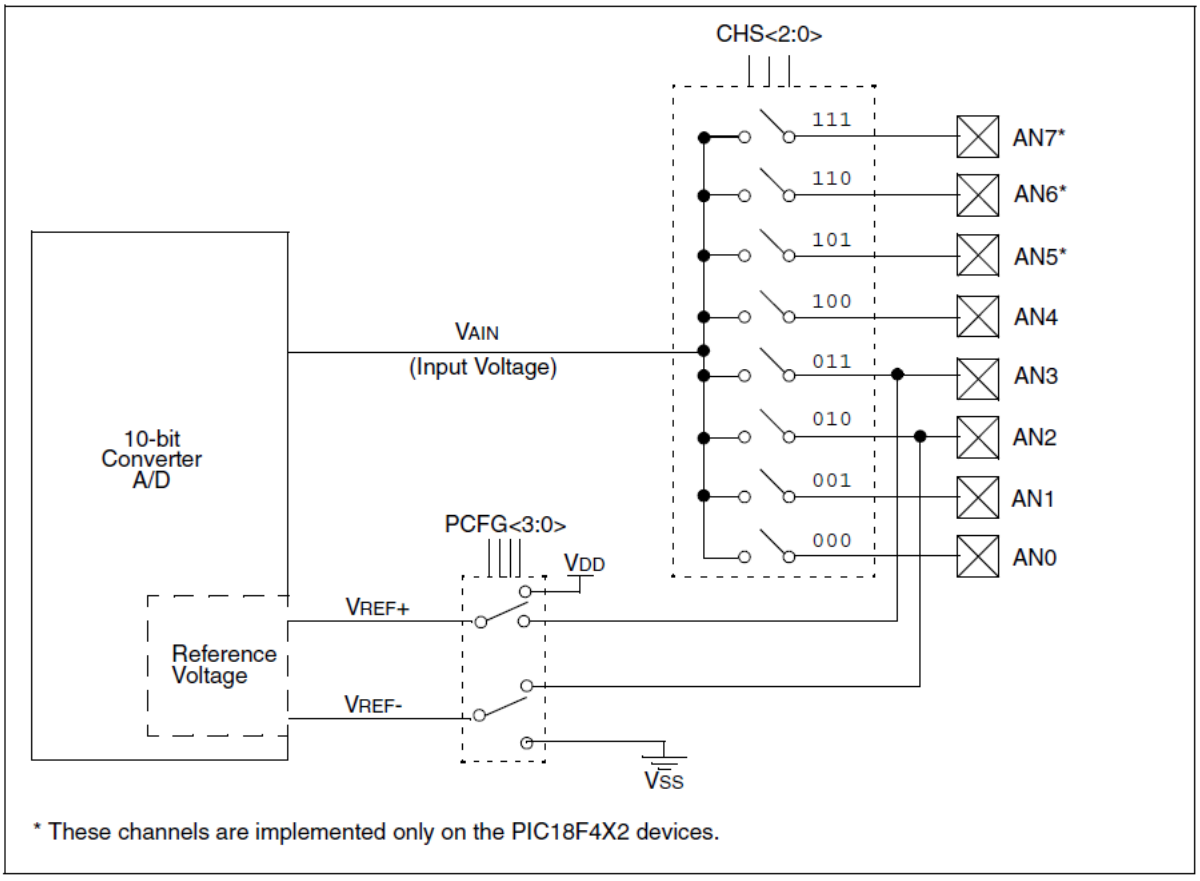

Figure 5: ADC Block diagram

Please turn the page…

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	FOSC/2
0	**01**	FOSC/8
0	**10**	FOSC/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	FOSC/4
1	**01**	FOSC/16
1	**10**	FOSC/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits
000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit
1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Figure 6: ADCON0 Register

Please turn the page…

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	FOSC/2
0	01	FOSC/8
0	10	FOSC/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	FOSC/4
1	01	FOSC/16
1	10	FOSC/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C / R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8 / 0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7 / 1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5 / 0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4 / 1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3 / 0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2 / 1
011x	D	D	D	D	D	D	D	D	—	—	0 / 0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6 / 2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6 / 0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5 / 1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4 / 2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3 / 2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2 / 2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1 / 0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1 / 2

A = Analog input D = Digital I/O
C/R = # of analog input channels / # of A/D voltage references

Figure 7: ADCON1 Register

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