[ESS017]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER 2 EXAMINATION 2018/2019

INTERMEDIATE DIGITAL ELECTRONICS AND COMMUNICATIONS

MODULE NO: EEE5012

Date: Wednesday 22nd May 2019 **Time: 14:00 – 16:30**

INSTRUCTIONS TO CANDIDATES: **There are FIVE questions.**

Answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

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Question 1

a) Simplify the following Boolean Algebra;
   (i) F = $\prod$ (1,5)
   (ii) F= $1 \oplus (AB)$

(4 marks)

b) Implement the F= $ABC + C\overline{D}$ using;
   (i) NAND gates only
   (ii) NOR gates only.

(6 marks)

c) By using five variable K –maps simplify;
   F = $\sum(1,2,5,6,7,8,9,10,13,17,18,21,22,29)$

(15 marks)

Total 25 marks

Question 2

a) A logic circuit is shown in **Figure 1**, simplify this circuit and show what single logic gate could replace this circuit. **(10 marks)**
b) If the NAND gates shown, were replaced by NOR what logic function would the circuit become. **(10 marks)**
c) Simplify f = $x \oplus \overline{x}\, y \oplus y$ **(5 marks)**

Total 25 marks

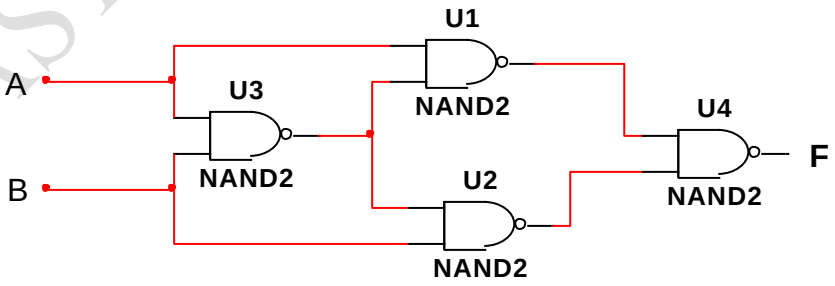

Figure 1

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Question 3

a) Determine the output states for this S-R flip-flop, given the pulse inputs shown in **Figure 2**: **(5 marks)**

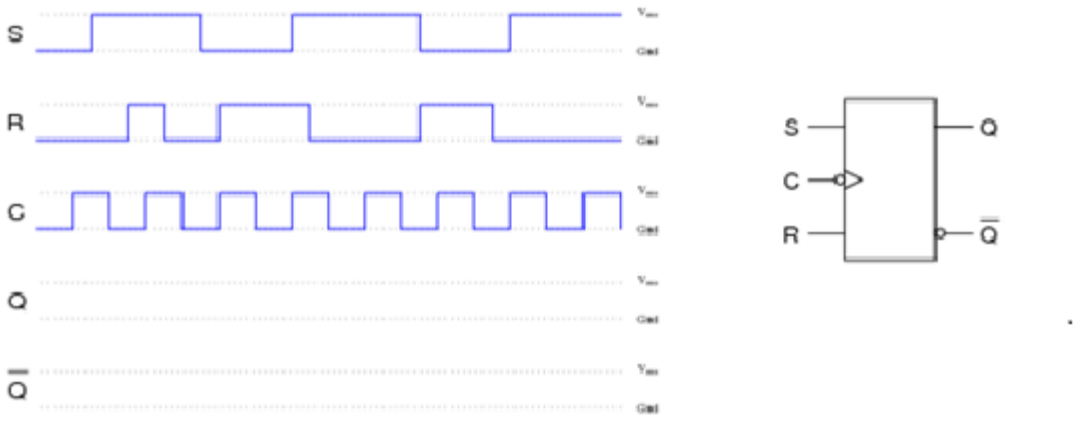

Figure 2

b) Determine the output states for this J-K flip-flop, given the pulse inputs shown in **Figure 3**. **(5 marks)**

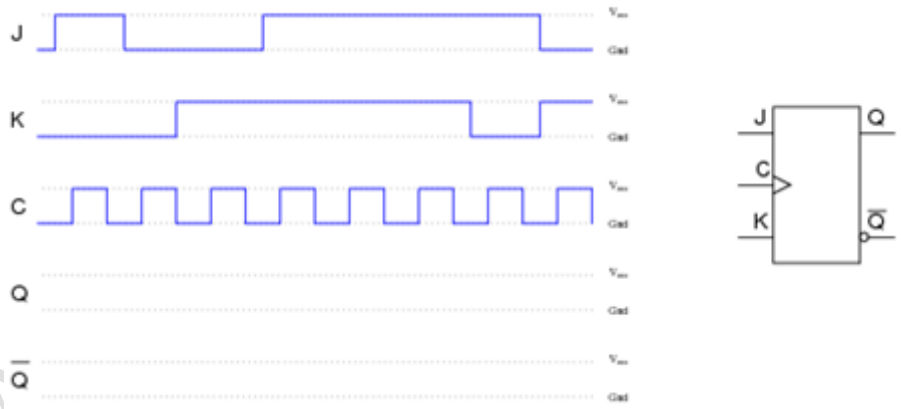

Figure 3

c) Design a Moore sequence detector, which generates a pulse when the embedded sequence 101 has occurred. **(15 marks)**

Total 25 marks

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Question 4

a) Describe how an Analogue to digital convertor can be constructed using a Digital to Analogue convertor.

(6 marks)

b) Explain the operation of Successive Approximation ADC, comparing the speed and accuracy with the counter ramp. **(6 marks)**

c) Sketch a four bit R-2R ladder D-A and describe it's operation. **(6 marks)**

d) If an R-2R ladder D-A has all eight bits set to logic one and Vref is 5volts, calculate the value of R_f to give an output voltage of -9.96 volts. **(7 marks)**

Total 25 marks

Question 5

a) Describe the main differences between the following PLD devices, PROM, PLA,PAL and GAL, illustrate your answers with a suitable diagram. **(8 marks)**

b) By completing the first column for the seven segment code shown in **Figure 4**,**(found on page 5)** derive a simplified expression for segment 'a' using a k-map and indicate on the PLD the fuse connections to generate the logic for segment 'a', **use Figure 6. (found on page 6)**

(8 marks)

c) For the PLD device shown in **Figure 5 (found on page 5)** derive the Boolean algebra for the two functions given. Simplify the equations and state the function. **(8 marks)**

d) If the gates G1and G2 have pin 2 connected to the supply how would the output function change.

(1 mark)

Total 25 marks

END OF QUESTIONS

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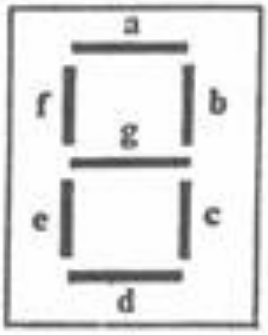

(*a*) Seven segment display

BCD	Segment (ON = 1)						
ABCD	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	1	1	0	0	0	0	0
0010	1	0	1	1	0	1	1
0011	1	1	1	0	0	1	1
0100	1	1	0	0	1	1	1
0101	0	1	1	0	1	1	1
0110	0	1	1	1	1	1	1
0111	1	1	0	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	0	0	1	1	1
1010	x	x	x	x	x	x	x
1011	x	x	x	x	x	x	x
1100	x	x	x	x	x	x	x
1101	x	x	x	x	x	x	x
1110	x	x	x	x	x	x	x
1111	x	x	x	x	x	x	x

(*b*) Partially completed truth table

Figure 4

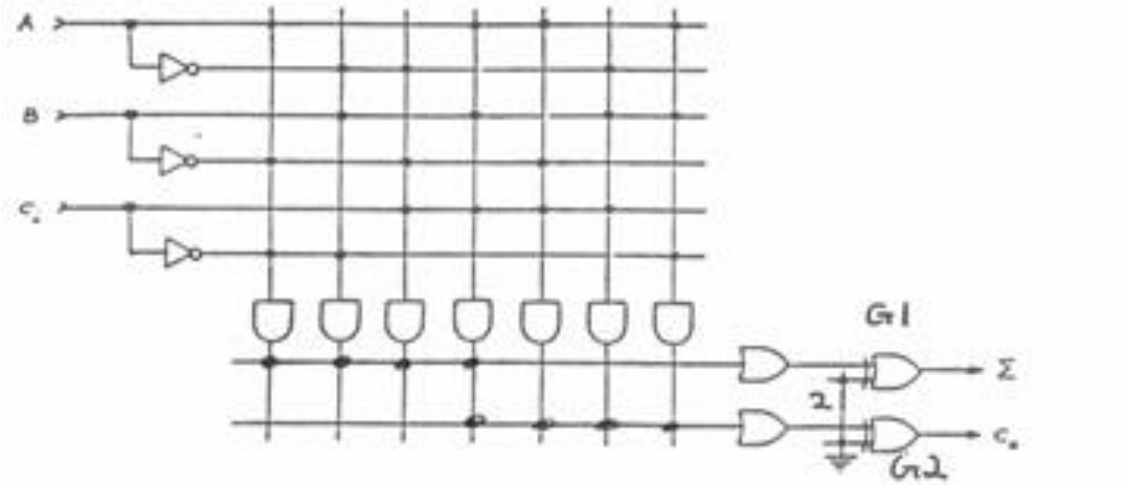

Figure 5

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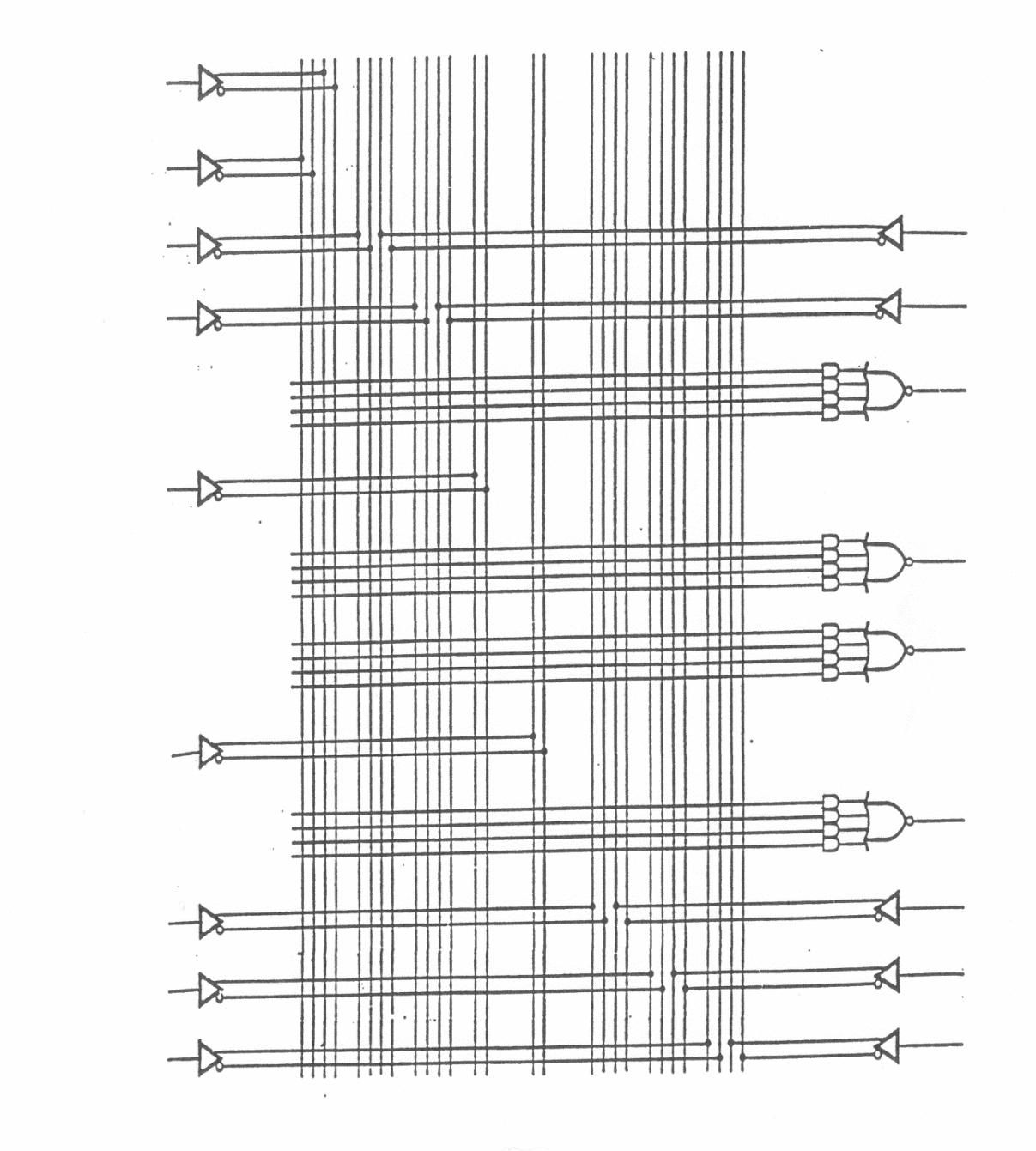

Figure 6

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