[ESS015]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

B.ENG (HONS) ELECTRICAL & ELECTRONICS ENGINEERING

EXAMINATION SEMESTER 2 - 2018/2019

INTRODUCTORY ANALGOUE ELECTRONICS

MODULE NO: EEE4014

Date: Wednesday 22nd May 2019 **Time: 10:00am – 12:00pm**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

Answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Electronic calculators may be used provided that data and program storage memory is cleared prior to the examination.

CANDIDATES REQUIRE:

Formula Sheet (attached).

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Q1

(a)

What is the graphical Volt-ampere characteristic plot of the normal silicon diode and ideal- diode model?

(10 marks)

(b)

Use the ideal-diode model to analyse the circuit as shown in Fig.1(b) to decide the working status of diode D1 and D2. (Please analyse all possible situations with **proper equivalent circuit** for both two diodes).

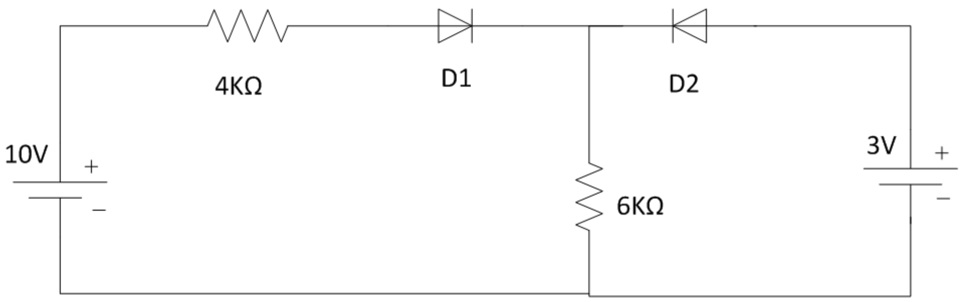

Fig.1(b) Diode circuit model

(15 marks)

Total 25 marks

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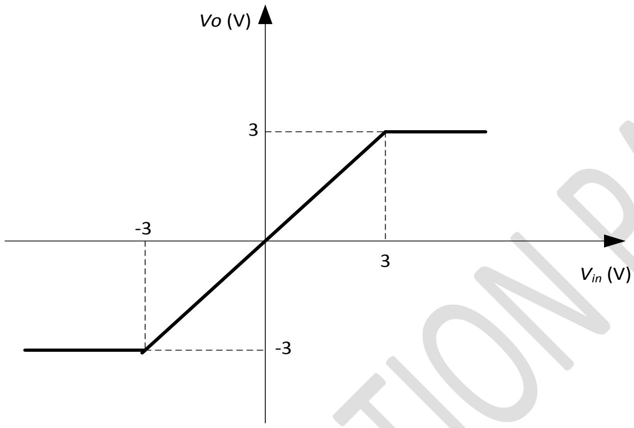
Q2.

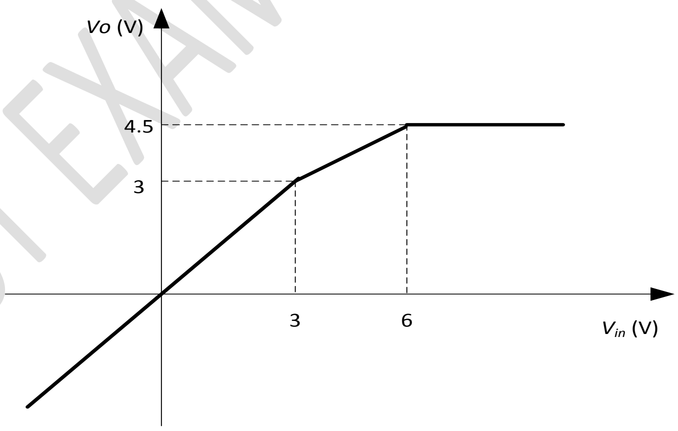
Using diode or Zener Diode to Design clipper circuits that have the transfer characteristics shown below if 0.6 V drop in the forward direction of diode is set.

(a)



(10 marks)

(b)



(15 marks)

Total 25 marks

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Q3.

(a) A certain **noninverting** amplifier has a voltage-gain magnitude of 100. The input voltage is $Vi(t) = 0.5\sin(2000\pi t)$. What is the expression for output voltage V_o(t) ?

(5 marks)

(b) If the amplifier is an **inverting** amplifier, repeat the question to find the expression of output voltage V_o(t).

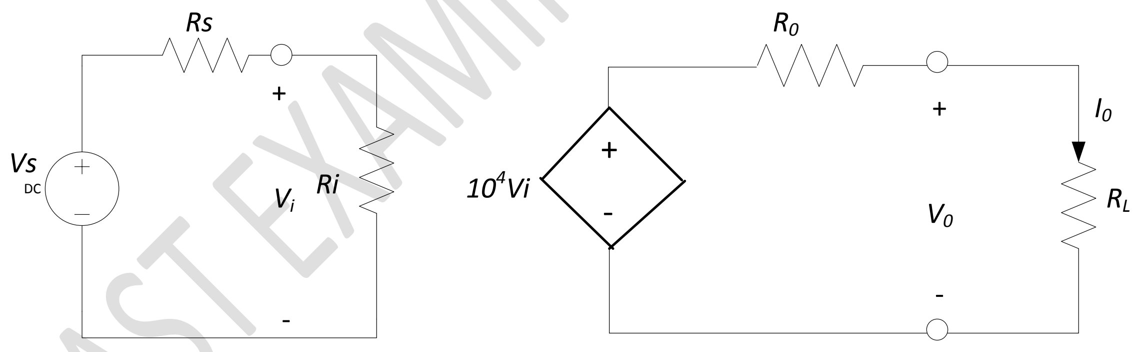
(4 marks)

(c) A source with an internal voltage of V_s = 1 mV and an internal resistance of R_s = 1 MΩ is connected to the input terminals of an amplifier having an open-circuit voltage gain of Av_{oc} = 10^4, an input resistance of R_i = 2 MΩ, and an output resistance of R_0 = 2 Ω, the load resistance R_L = 8Ω.

Find i) Voltage gain $A_{vs}=V_0/Vs$ and $A_v = V_0/Vi$.

ii) Current gain. Note: $A_i = A_v R_i / R_L$.

iii) Power gain. Note: $G = A_v A_i$



(16 marks)

Total 25 marks

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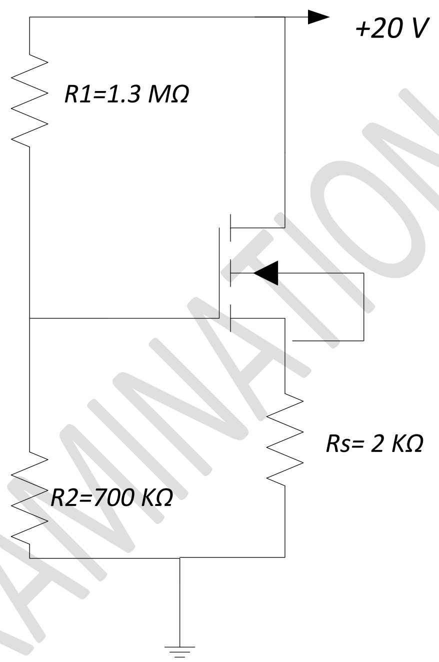
Q4.

Analyse the fixed-plus self-bias circuit shown below and determine I_{DQ} and V_{DSQ} for the circuit. The FET transistor has KP= 50 $\mu A/V^2$, V_{to}=1 V, L= 10 μm and W=200 μm. Please draw the Thevenin equivalent circuit to help the solution.

Note: $K = \frac{w}{L}\frac{KP}{2}$; $I_D = K(V_{GS} - V_{to})^2$



(25 marks)

Total 25 marks

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Q5.

Analyse the Four-Resistor Bias BJT transistor Circuit as shown in Fig.Q5.

(a) Determine the value of I_C and V_{CE} for the circuit for β=100 and β=300.

(16 marks)

(b) Draw the corresponding Thevenin Equivalent Circuit and the equivalent Large-Signal DC circuit model.

(9 marks)

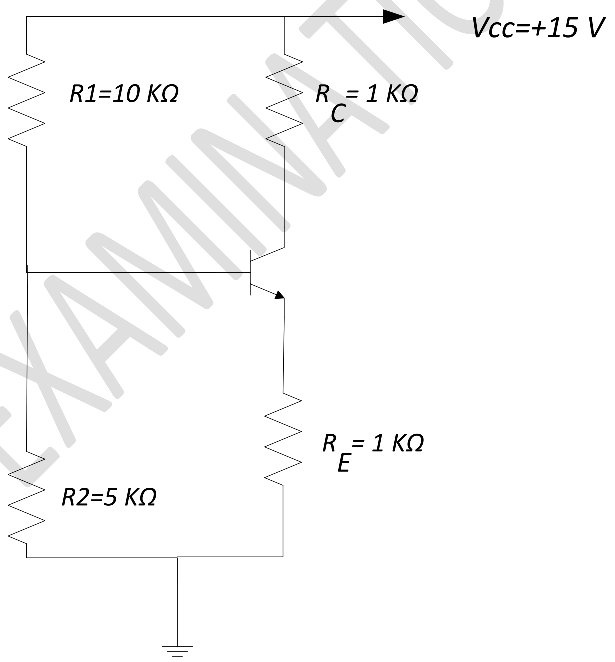

Fig. Q5: A BJT Transistor Circuit

Total 25 marks

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Q6.

a) An operational amplifier has high input impedance and low output impedance. Briefly explain why this is desirable.

(6 marks)

b) Fig.6b is a diagram of a summing inverting negative feedback operational amplifier circuit with two inputs V1 and V2 and an output Vo. What is the value of Vo if V1=1.5V and V2 = 2.5V ?

(4 marks)

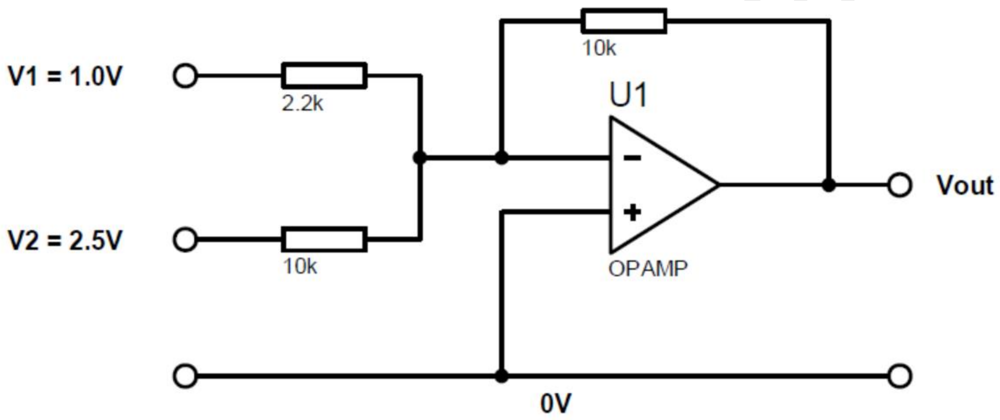

Fig.6b: Summing amplifier (has a supply of +/- 12 V)

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Q6 continued…

c) Determine the input voltage (V_{in1}) from a cascaded operational amplifier circuit as shown in Fig.Q6c.

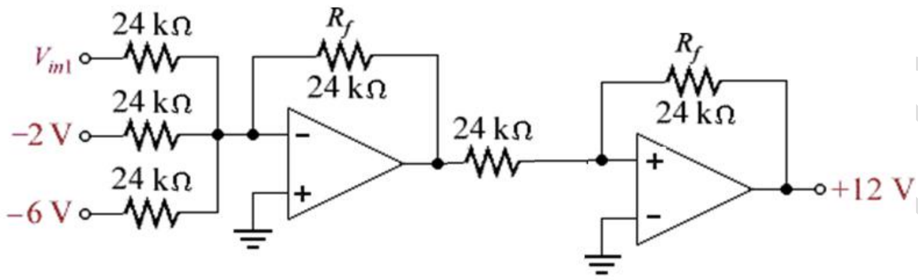

Fig.Q6c: A cascaded operational amplifier circuit.

(7 marks)

d) Briefly define the term common mode rejection ratio. An amplifier has a CMRR of 75 dB. Restate this CMRR as an arithmetic ratio e.g. *x*:1, where *x* is a numerical value.

(8 marks)

Total 25 marks

END OF QUESTIONS

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Formula sheet

These equations are given to save short-term memorisation of details of derived equations and are given without any explanation or definition of symbols; the student is expected to know the meanings and usage.

Ohms law: $V=RI$

Power : $P= IV$

Voltage divider: $V_{Ri}=V_S(R_i/(R_i+R_S))$

Current gain: $A_i=I_o/I_i$

Power gain: $A_P=P_o/P_i=V_oI_o/V_iI_i = A_vA_i$

Bipolar Transistor:

$I_E=I_B+I_C= (\beta+1)\ I_B$

$I_C=\beta I_B$

$r_\pi = V_T/I_B$, where $V_T=0.026V$

$$I_E = (\beta + 1)I_B$$

$$I_B = \frac{V_{B-V_{BE}}}{R_{B+}(\beta + 1)R_E}$$

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MOSFET:

$V_G=(R_2/(R_1+R_2))*V_D$

$V_G= V_{GS}+R_S I_D$

$I_D=K(V_{GS}-V_t)2$

$V_{DS}=V_{DD} - (R_D+R_S)*I_D$

$K = \frac{w}{L}\frac{KP}{2};\ \ I_D = K(V_{GS} - V_{to})^2$

Operational Amplifier:

$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_a}$ ------------- Non-inverting

$V_o = -R_f\left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right) = -R_f\sum_{j=a}^{c}\frac{V_j}{R_j}$ ------------- Multiple Inputs

$\frac{V_o}{V_{in}} = \frac{-R_f}{R_a}$ ------------- Inverting

Diode:

$V_r = \frac{V_M}{2fRC}$

$$Duty\ cycle = \left(\frac{\theta_2 - \theta_1}{2\pi}\right)$$

END OF FORMULA SHEET

END OF PAPER