[ESS12]

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

BENG (HONS) ELECTRICAL AND ELECTRONIC ENGINEERING

SEMESTER TWO EXAMINATION 2018/2019

INTRODUCTORY DIGITAL ELECTRONICS

MODULE NO: EEE4013

Date: Monday 20th May 2019 **Time: 14:00 – 16:00**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

Answer ANY FOUR questions.

All questions carry equal marks.

Individual marks are shown within the question.

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Q1 a) What is the difference between the Gray code and Binary code? Provide an example of where the Gray code can be used.

[2 marks]

b) Show how the binary code, 1100110, can be converted to its equivalent Gray code.

[3 marks]

c) Perform the following arithmetic operations. Please note carefully the radix (base) of the number system:

(i) $2A_{16} + 6B_{16} = XX_{10}$ **[5 marks]**

(ii) $1101_2 \times 1101_2 = XX_{10}$ **[5 marks]**

d) Complete the missing entries, **which are not shaded,** in the following figure Q1d. Please show all the steps that lead to the solution.

Hexadecimal	Binary	Decimal
	11010	?
	?	33
	?	105
A2	?	?

Fig. Q1d

[10 marks]

Total 25 marks

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Q2 a) For each circuit in figure Q2a below, determine if the LED should be on or off. Also provide the rationale behind your answer as well.

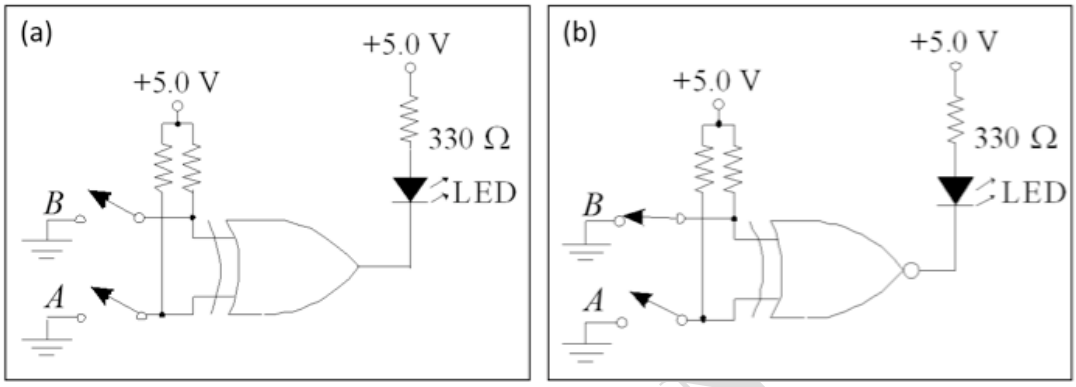

Fig.Q2a: Digital circuits with LED

[4 marks]

b) Simplify the following Boolean expression using Boolean algebra and/or De Morgan's theorem.

$$X = \overline{(\bar{A} + A\bar{B})} + C\overline{(A + \bar{A}B)}$$

[5 marks]

c) For the circuit shown in Fig. Q2c, construct a Truth Table for the logical functions at points C, D and Q. From the truth table obtained, identify a single logic gate that can be used to replace the complete circuit.

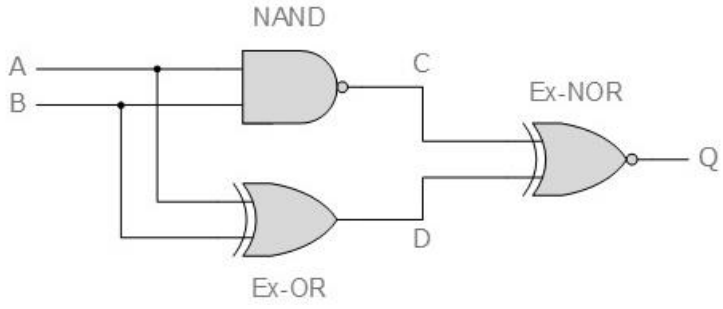

Fig. Q2c: A two input digital circuit

[6 marks]

Question 2 continues over the page….

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Question 2 continued….

d) Using a Karnaugh map, convert the following expressions to a minimised SOP (sum-of-product) form:

(i) $X = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C}D + A\overline{C}\,\overline{D} + A\overline{C}D + A\overline{B}C\overline{D}$

(ii) $X = \overline{A}\,\overline{B} + A\overline{B}\,\overline{C} + A\overline{B}C + ABC$

[10 marks]

Total 25 marks

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Q3 a) For the circuit shown below (**Fig. Q3a**), the J-K inputs for both the flip-flops are tied to HIGH.

(i) With the help of appropriate waveforms, draw and describe the outputs from Q_A and Q_B (f_{out}).

[5 marks]

(ii) If the input frequency (f_{in}) has a clock frequency of 50 MHz what will be values of the frequencies available at Q_A and Q_B?

[5 marks]

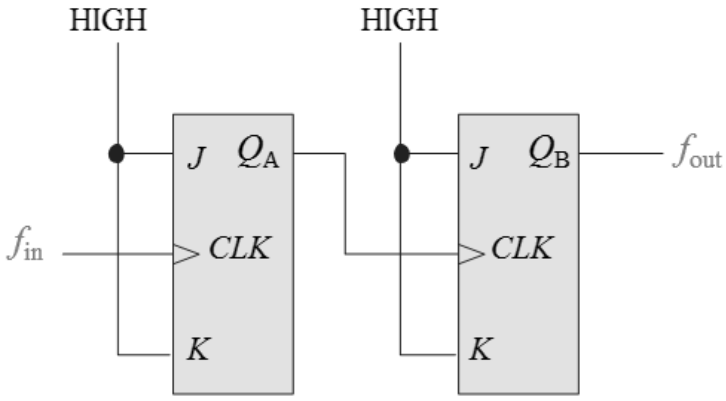

Fig.Q3a: J-K flip flop circuit

b) Determine the input conditions needed to produce x= 1 for the circuit below (**Fig.Q3b**):

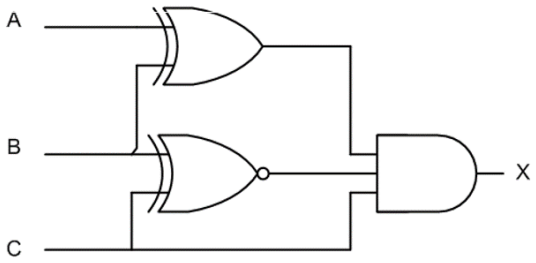

Fig. Q3b: Digital circuit

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[5 marks]

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Question 3 continued….

c) Assuming the output of the decoder shown below (**Fig. Q3c**) is a logic "1". What are the inputs to the Active HIGH decoder and the logic expression of the decoder?

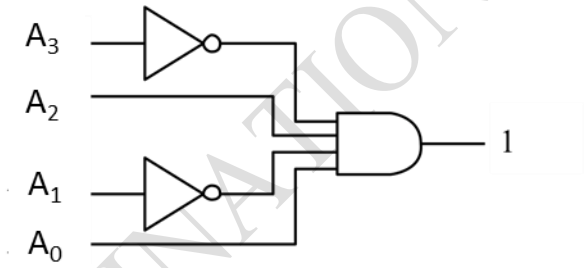

Fig. Q3c: a logic gate circuit

[5 marks]

d) Determine the sum generated by the 8-bit parallel adder shown in **Fig.Q3d** below and show the intermediate carries when binary numbers A=10010110 and B= 10110011 are added.

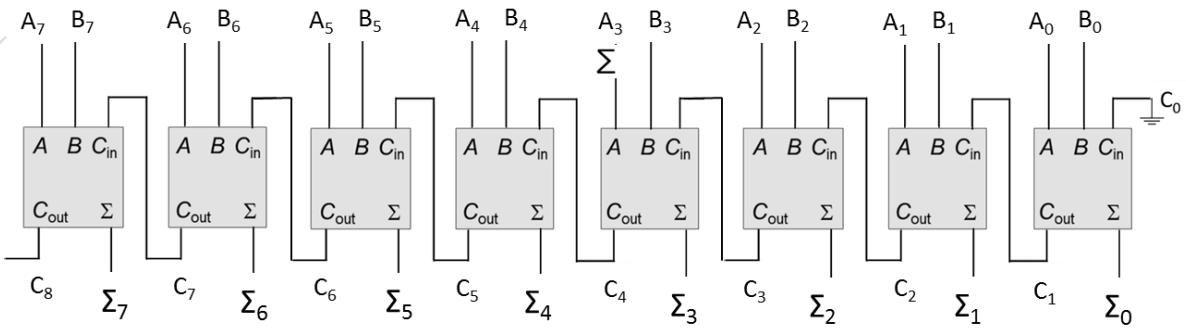

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Fig. Q3d: 8-bit parallel adder

[5 marks]

Total 25 marks

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Q4 a) For an active HIGH input S-R latch being controlled by the S, R signals in the manner shown below (**Fig.Q4a**), draw the output signal showing the variation in the state of the output Q, assuming it is initially LOW.

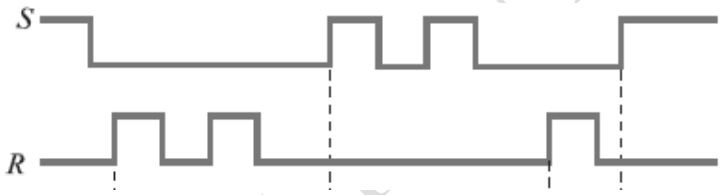

Fig. Q4a: Input wave form for a S-R latch

[5 marks]

b) It is often useful to be able to control the operation of a latch so that the inputs can be enabled (EN) at some times and disabled at others. Given a gated D-latch being controlled by the D and EN signals (**Fig.Q4b**), show the variation in the state of the output Q, assuming that Q is starting LOW.

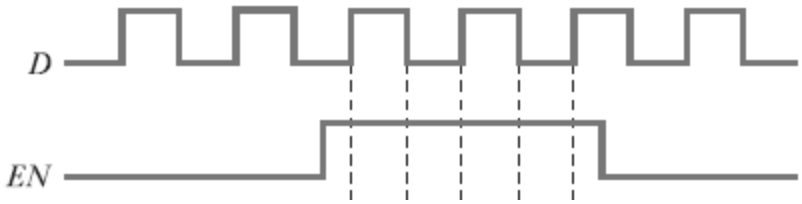

Fig. Q4b: Input wave form for a gated D-latch

[5 marks]

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c) For a 1-bit half adder incorporating A, B and C_{in} as the input signals and S and Co as the output signals, you have been asked to reduce the number of logic gates in the circuit by utilizing multiplexers. Utilizing two 4:1 Mux, design a 1-bit full adder.

[10 marks]

Question 4 continues over the page….

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Question 4 continued….

d) For a negative-edge triggered J-K flip-flop being controlled by the following J, K signals (**Fig. Q4d**), show the variation of the output state Q, assuming Q is starting HIGH.

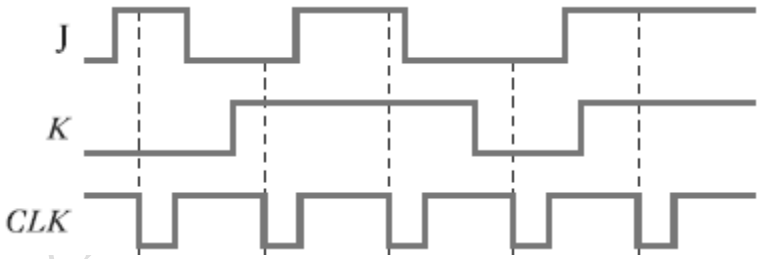

Fig.Q4d: Input waveform for J-K flip-flop

[5 marks]

Total 25 marks

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Q5 a) For the 5-bit register, show its states for the specified data input and CLK waveforms as shown in Fig. Q5a. Assume that the register is initially cleared.

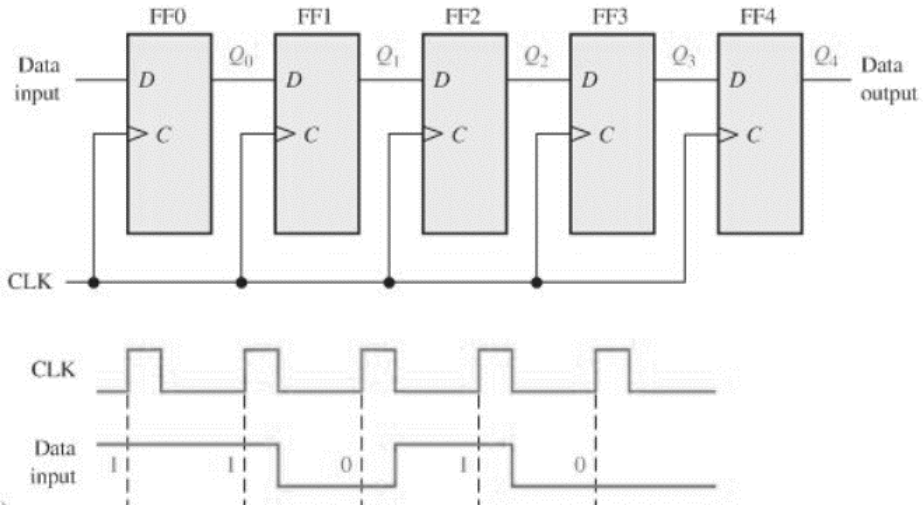

Fig. Q5a: 5 bit register

[7 marks]

b) For the BCD decade counter shown below (Fig. Q5b), assuming the J0 and K0 inputs are tied HIGH, draw the output waveforms for Q0, Q1, Q2 and Q3.

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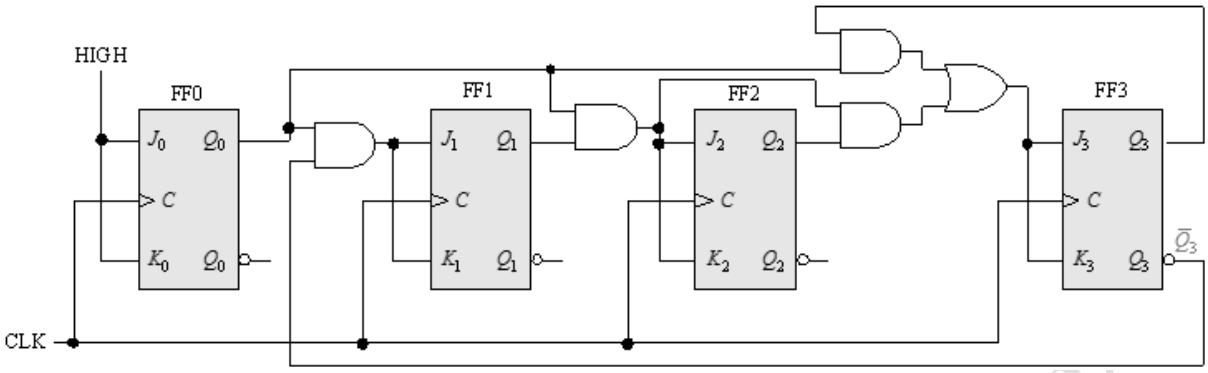

Fig. Q5b: BCD decade counter

[10 marks]

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Question 5 continued….

c) Using J-K flip-flops, design a 2-bit asynchronous counter and show its corresponding output waveforms.

[8 marks]

Total 25 marks

Q6 a) Explain the difference between combinational and sequential circuits.

[2 marks]

b) Explain the difference between latches and flip flops. **[2 marks]**

c) A circuit has four inputs and two outputs. The inputs, A3:0, represent a number from 0 to 15. Output P should be TRUE if the number is prime (Hint: A number is prime if it is divisible only by itself and 1; 1 is considered to be prime, and 0 is not). Output D should be TRUE if the number is divisible by 3.

(i) Give simplified Boolean equations and Truth Table for each of the outputs P and D. **[12 marks]**

(ii) Construct the circuit that takes these 4 inputs (A3:0) and produces the output P. **[4 marks]**

d) Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1. Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates. **[5 marks]**

Total 25 marks

END OF QUESTIONS