UNIVERSITY OF BOLTON

RAK ACADEMIC CENTRE

B.SC. (HONS) COMPUTING

SEMESTER TWO EXAMINATION 2018/2019

COMPUTER PLATFORMS

MODULE NO: CPU4004

Date: Thursday 23rd May 2019   **Time: 1:00pm – 3:00pm**

INSTRUCTIONS TO CANDIDATES:

Answer all questions in section A and any three questions in section B.

Each question in section A carry 1 mark

All questions in section B carry equal marks.

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

SECTION A – Answer all questions

Q1.

This is a multiple choice question consisting of 20 parts each carrying **1 mark**. Each part has four possible answers of which ONLY ONE is correct.

To indicate your selection, write the question number and your answer in the answer book.

i. Valid and unimpeachable measurement of performance of any computer is

    a. Clock rate

    b. Instruction set

    c. Execution time

    d. Delay time

ii. *Performance = 1/ Execution Time*, given relation shows that

    a. Performance is increased when execution time is decreased

    b. Performance is increased when execution time is increased

    c. Performance is decreased when execution time is decreased

    d. None

iii. Total amount of work done during execution, in a given time is referred to as

    a. Response time

    b. Execution time

    c. Through put

    d. Delay time

iv. FAT stands for

    a. File Accommodation Table

    b. File Access Tape

    c. File Allocation Table

    d. File Activity Table

Q1 Continued over the page

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q1 continued.

v. The priority of a process will _____, if the scheduler assigns it a static priority

    a. change

    b. remain unchanged

    c. depends on the operating system

    d. None of these

vi. Nodes are another name of

    a. Devices

    b. Links

    c. Medium

    d. Modes

vii. In Linux what command is used to remove files?

    a. dm

    b. rm

    c. delete

    d. erase

viii. Which scheduling algorithm allocates the CPU first to the process that requests the CPU first?

    a. first-come first-served scheduling

    b. shortest job scheduling

    c. priority scheduling

    d. none of the mentioned

ix. The average time required to reach a storage location in memory and obtain its contents is called the

    a. seek time

    b. turnaround time

    c. access time

    d. transfer time

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q1 continued.

x.   Which of the following is lowest in memory hierarchy?

    a. Cache memory

    b. Secondary memory

    c. Registers

    d. RAM

xi.   The circuit used to store one bit of data is known as

    a. Register

    b. Encoder

    c. Decoder

    d. Flip Flop

xii.   Cache memory acts between

    a. CPU and RAM

    b. RAM and ROM

    c. CPU and Hard Disk

    d. None of these

xiii.   What characteristic of RAM memory makes it not suitable for permanent storage?

    a. Too slow

    b. Unreliable

    c. It is volatile

    d. Too costly

xiv.   Combination of two or more topologies are

    a. Star Topology

    b. Bus Topology

    c. Ring topology

    d. Hybrid

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q1 continued.

xv.   Which of the following registers is used to keep track of address of the memory location where the next instruction is located?

     a. Memory Address Register

     b. Memory Data Register

     c. Instruction Register

     d. Program Counter

xvi.   What will be the binary representation for 777?

     a. 10011111

     b. 10000100

     c. 1100001001

     d. None of the above

xvii.   What is the decimal conversion for 11001100?

     a. 115

     b. 204

     c. 240

     d. 101

xviii. Which one of the following is not an operating system?

     a. MacOS

     b. RTOS

     c. MSDOS

     d. Java

xix.   Which one of the following is the address generated by CPU?

     a. physical address

     b. absolute address

     c. logical address

     d. none of the mentioned

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q1 continued.

xx.   If a 2-input NAND gate has four input possibilities, how many of those possibilities will result in a HIGH output?

     a. 1

     b. 2

     c. 3

     d. 8

Total 20 marks

SECTION B - Answer any three questions.

Q2.

i.   Define

     a. Pre-emptive scheduling

(1.5 marks)

     b. Non pre-emptive scheduling

(1.5 marks)

     c. Threads

(1.5 marks)

     d. Process

(1.5 marks)

ii.   Draw a diagram which explains the instruction execution cycle for the instruction 'Sub R1,R2'.

(6 marks)

iii.   Discuss internal and external fragmentation with the help of an example diagram.

(8 marks)

Total 20 marks

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q3.

i. What is an interrupt? Explain interrupt with the help of a neat sketch.

(6 marks)

ii. Briefly describe storage hierarchy with the aid of a diagram.

(8 marks)

iii. Explain

a. Program Counter (PC)

(1.5 marks)

b. Memory Address Register (MAR)

(1.5 marks)

c. Instruction Register (IR)

(1.5 marks)

d. Arithmetic and Logic Unit (ALU)

(1.5 marks)

Total 20 marks

Q4.

i. Explain various pieces of information associated with Process Control Block with a diagram.

(7 marks)

ii. Discuss any 2 CPU scheduling algorithms with an example.

(6 marks)

iii. Using the concept of virtual memory, explain swapping of two processes with a diagram.   .

(7 marks)

Total 20 marks

University of Bolton
RAK Academic Centre
B.Sc. (Hons) Computing
Semester 2 Examination 2018/2019
Computer Platforms
Module No. CPU4004

Q5.

i. What are the different states of a process, explain with a diagram.

(6 Marks)

ii. Draw and explain the Von Neuman and Harvard architecture.

(8 Marks)

iii. Draw computer architecture diagram for MISD and SIMD.

(6 Marks)

Total 20 marks

END OF QUESTIONS